

SIMULATION STUDY OF SHORT CHANNEL EFFECTS IN LOW POWER FINFETS WITH DIFFERENT BODY SHAPE AND GEOMETRIES

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One of the ways to reach low power consumption in semiconductor devices is the decreasing sizes. Metal-oxide-semiconductor field effect transistor (MOSFET) scaling induces different effects that tend to degrade device performance. Among them more important ones is technological variability of parameters and short channel effects (SCEs). One of types of variability is the narrowing of the body which might appear in multiple-gate vertical field effect transistor (FinFET). In this work, short channel effect such as drain induced barrier lowering (DIBL) and sub threshold swing (SS) is compared for silicon on insulator (SOI)-FinFETs with different silicon body shapes and geometries. It was considered the original device, which is straight without narrowing at the top and a set of devices that exhibit the mentioned narrowing, up to the extreme case where the top of the gate has no surface and so the body cross-section is a triangle. We have studied five different variations from the original geometry of a 25 nm gate length SOI-FinFET device with oxide thickness 1.5 nm. P-type channel has doping concentration of 10^{15} cm^{-3} and n-type S/D areas are doped with concentrations of 10^{20} cm^{-3} . Silicon body of the device has height and width of 30 nm and 12 nm accordingly. Simulation results show DIBL effect as well as SS of the considered FinFETs depends on body top thickness and is increased with increasing of the body top thickness. Thickness of back oxide (BOX), gate oxide overlapping and extension of gate width influence to DIBL and SS. DIBL and SS is increased with increasing the BOX thickness, while DIBL is decreased with increasing the length of BOX. With extension of the gate, DIBL as well as SS is decreased

Biography

Azamat Abdikarimov has completed his BS and MS diploma in Physics in 2004 and 2006 correspondingly from Urganch State University. He is the PhD student at Physics department of Urganch State University. In 2012-2014, he had conducted researches in the group of Computational Electronics in University Santiago de Compostella (Spain). He has published 4 papers in reputed journals. At Urganch State University, he is Member of the group of electronics and modelling of semiconductor devices and participates in several national and international research projects. He is Advisor for 4 BS students at the Physics department of Urganch State University.

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