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The Effect of Modified PVA Interfacial Layer Doped by Zn Nanoparticles on the Electrical Parameters of Au/N-4H Sic (MS) Structures

Al-Dharob MH[1], Kökce A[1]*, Lapa HE[1], Özdemir AF[1] and Altındal S[2]

1 Department of Physics, Faculty of Arts and Sciences, Süleyman Demirel University, Isparta, Turkey
2 Department of Physics, Faculty of Sciences, Gazi University, Ankara, Turkey

***Corresponding author:** Kökce A

alikokce@sdu.edu.tr

Department of Physics, Faculty of Arts and Sciences, Süleyman Demirel University, Isparta, Turkey.

Tel: 2462114031

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Abstract

Both Au/n-4H SiC (MS) and Au/(Zn doped-PVA)/n-4H SiC (MPS) structures were fabricated by using the same wafer. This effect of modified PVA interlayer doped by Zn nanoparticles on main electrical parameters, such as ideality factor (*n*), barrier height (BH), series resistance (R_s), and rectification rate (*RR*) were evaluated and investigated by using the current-voltage (*I-V*) data measurements. Furthermore, the energy dependent profile of surface states (N_{ss}) was also obtained from these data by taking into account voltage dependent BH and n. The sources of observed negative capacitance (NC) at the accumulation region for the MS and MPS structures were also evaluated. From capacitance-voltage (*C-V*) and conductance-voltage (G/ω-*V*) data measurements, the profile of R_s and N_{ss} were also evaluated and investigated as voltage dependent at high frequency (1 MHz) by using Nicollian-Brews technique. These results explain how is the effect of modified PVA interfacial layer doped by Zn nanoparticles on increasing in the RR and decreasing of the values of R_s, N_{ss}, and leakage current of MPS structure as compared with MS structure. Thus, we can say that this increase in the performance of the MPS structure is a result of the grown of the (Zn-doped PVA) layer between Au and n-4H SiC.

Keywords: MS and MPS structures; Passivation effect; Surface states; Negative capacitance

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Introduction

Recently, many of experimental researches and studies for the metal-polymer-semiconductor (MPS) type structures in order to replacing the traditional metal-semiconductor (MS) structures with and without insulation interfacial layer such as SiO_2 or SnO_2 [1-7]. In general, pure polymer usually is a poor conductivity material, but its conductivity can be increased by using doping with a metal at appropriate rates [8-11]. Therefore, polymer interfacial layers attract considerable attention in the electronic and optoelectronic devices due to their easy device fabrication, flexibility, low cost, suitability.

There are different kinds of polymers/organics among of them is poly (vinyl alcohol) (PVA) that has a semi-crystalline structure and high water-solubility, nontoxic, crystallinity with wide range, good charge/energy storage capacity and high dielectric strength properties [12-15].

In addition, PVA is from hydroxyl group; therefore it can be reacts easily with other organic and inorganic compounds. Therefore, in very recently, it is believed that MPS structure is considered one of the most promising candidates in the future semiconductor technology instead of classic/conventional MS, MOS and MIS type structures [8-15].

At the same time, silicon carbide (SiC) represents a very important semiconductor among many kinds of semiconductor crystals with wide band-gap (E_g) [16]. Furthermore, SiC is 3 times wider E_g (=3.2 eV) and 10 times higher critical electric field (E=2.2 × 10^6 V/cm) when compared conventional Si semiconductor [17].

It is clear that the electrical properties of MS structure with exist of insulator or organic interfacial layer and without it usually not only depend on the metal and interfacial layer used, but depend strongly on the surface properties, doping concentration level of semiconductor, barrier form at the interface between metal

and semiconductor, series and shunt resistances of the device (R_s and R_{sh}) and applied bias voltage across the junction [18-26]. Especially, high-dielectric interlayer can cause the leakage reverse current, n, R_s and N_{ss}, and increase the BH, intercept voltage (V_i or V_o) and R_{sh} [27]. Zinc (Zn), Cobalt (Co) and nickel (Ni) were used as doped materials due to low cost, abundant raw material and heat cycling. The other more important feature of the SiC is the ability to form SiO_2 as a native insulator/oxide layer. There are still a number of factors which are limiting the device performance such as the formation of back Ohmic contact with low resistivity and high-temperature stable Schottky/rectifier contacts. Both Zn and SiC have also the same wurtzite crystal symmetry and relatively higher lattice mismatch (5%). Although there are various "poly-types" SiC, but the most preferred among is 4H-SiC due to its superior physical properties through owing double electron mobility as compare with 6H-SiC at a given dopant density and the availability of high-quality epitaxial wafers [27-30].

In this study, the experimental result give us a good indicate about how is the effect of modified PVA interfacial layer doped by Zn nanoparticles on electrical properties and conduction/transport mechanism, therefore, after we fabricate Au/n-SiC (MS) and Au/(Zn-PVA)/n-4H SiC (MPS) structures, we calculate and investigate the main electrical parameters for both structures to compare between them by using the forward and reverse bias *I-V*, *C-V* and *G/ω-V* measurements at room temperature. The interface state energy distribution profiles of N_{ss} were obtained from the forward bias *I-V* data for two type structures by taking into account voltage dependent BH and ideality factor. As a results of comparison between the two structures, it was found that the modified PVA interfacial layer doped by Zn nanoparticles leads to a decrease in the values N_{ss}, R_s, leakage current and increase in shunt resistance (R_{sh}) and *RR*.

Experimental Details

Au/n-4H SiC (MS) and Au/Zn-PVA/n-SiC (MPS) with modified PVA interfacial layer doped by Zn nanoparticles structures were fabricated by using two same quarter n-type 4H-SiC (0001) wafer with the following properties: donor concentration atoms (N_d) about 7.07×10^{17} cm^{-3}, rectifying contact area 0.0314 cm^2 and thickness about 250 µm. for fabrication process, firstly, n-type 4H-SiC wafer was dipped in organic solution of ammonium peroxide solution for 10 minutes to remove any oxide thin layer that could be cover it, and then etched in a sequence of acidic solution H_2O+HCl by using ultrasonic bath and then quenched in de-ionized water (DI) with 18 MΩ.cm resistivity for 10 minutes. Preceding each cleaning step, the wafer was rinsed thoroughly in DI water. Finally, n-4H SiC wafer dried in the high-pure dry nitrogen (N_2) gas to prevent any oxidation of the wafer and then high purity (99.999%) Au with 1500 Å thickness was thermally evaporated onto the whole back side of n type 4H-SiC wafer at 10^{-6} Torr in the metal evaporation system (MES). In order to perform a low resistivity Ohmic back contact, n-4H SiC wafer was sintered at 500°C for 5 minutes in the nitrogen ambient.

After the formation of ohmic contact, firstly, high purity Au dots with 0.0314 cm^2 and 1500 Å thickness was thermally evaporated onto the front of the first quarter n-4H SiC wafer in the same MES. By this way the fabrication processes of Au/n-4H SiC (MS) were completed. Secondly, the prepared (Zn-doped PVA) solution was deposited onto the front of the second quarter n-4H SiC wafer by using electrospinning method. Lastly, like the first sample high purity Au dots with 0.0314 cm^2 and 1500 Å thickness was also thermally evaporated onto the front of the second quarter and so on the fabrication processes of Au/Zn-PVA/n-SiC (MPS) structures were also completed. The metal thickness layer and the deposition rates were monitored with the help of quartz crystal thickness monitor. The schematic diagrams of the fabricated of MS and MPS type structures were given in **Figure 1a and 1b**, respectively.

In order to obtain the *I-V*, *C-V* and *G/-V* measurements for both MS and MPS structures, they were mounted on a copper (Cu) holder with the help of silver paste and electrical measurements were made to the upper electrodes by the use of tiny silver coated Cu-wires with silver paste. The measurement system was also given in **Figure 2**. The thickness of (Zn-PVA) (d_i) was determined as 50 nm from the high frequency (1MHz) C-V plot of the interlayer capacitance ($C_i=\varepsilon_{ro} A/d_i$) at the strong accumulation region. As shown in **Figure 2**, the *C-V* and *G/ω-V* measurements were performed by the use of a computerized HP 4192A LF impedance analyzer (5 Hz-13 MHz) at low (1 kHz) and high (1 MHz) frequencies. On the other hand, the I-V measurements were performed by the use of a Keithley 2400 I-V source-meter. In addition, all measurements were carried out in dark with the help of a microcomputer through an IEEE-488 AC/DC converter card in the JANES-475 Cryostat at about 10^{-3}Torr to avoid an external noise or other environmental effects **(Figure 2)**.

Results and Discussion

The forward and reverse bias current-voltage (I-V) characteristics

In order to determine whether or not a MS structure with modified PVA interfacial layer doped by Zn nanoparticles and without an interfacial layer has the ideal diode behavior, its experimental results at forward bias *I-V* characteristics and low or intermediate voltage ($V3kT/q$) can be analyzed according to thermionic emission (TE) theory [18-20].

$$I = \underbrace{AA^*T^2 \exp(-\frac{q\hat{O}_{B0}}{kT})}_{I_o}\left[exp\left(\frac{qV_D}{nkT}\right)-1\right] \quad (1)$$

The pre-factor or the first part of the eqn. (1) represent the saturation current (I_o) calculated from straight line intercept of *LnI* at V=0, A^* is the effective Richardson constant (146 $A.cm^{-2}K^{-2}$ for n-type 4H SiC, A is the rectifier/Schottky contact area, T is the absolute temperature in *K*, V_D is the voltage drop across the junction ad n is the ideality factor [19], and the other quantities are well known in the literature. **Figure 3** shows the experimental reverse and forward bias *I-V* characteristics for MS and MPS type structures at room temperature. As shown in **Figure 3**, both MS and MPS type structures have a rectifying behavior with exponential increase of the current showing in the forward bias and weak voltage dependence in the reverse bias regions. The

value of I_0 was evaluated from the intercept of the linear region of *LnI-V* plots, whereas the value of n was evaluated from its slope for both structures according to the following equation [18,19].

$$n = q / kT\left(\frac{dV}{d\left(lnI\right)}\right) = 1 + \frac{\delta_i}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\right] \quad (2)$$

Where, δ_i represent the thickness of interlayer, W_D represent the depletion layer width, N_{ss} represent the surface states/traps, ε_i and ε_s represents the permittivity of modified PVA interfacial layer doped by Zn nanoparticles and semiconductor, respectively.

Now, the value of Φ_{Bo} was calculated by using theoretical value of A^* and extrapolated I_o values as following equation for two type structures [20].

$$\hat{O}_{B0} = \frac{kT}{q}\ln(\frac{AA^*T^2}{I_0}) \quad (3)$$

Figure 3, Ln*I* vs. *V* plot of the MPS structure shows two linear regions with different slopes whereas for MS structure this plot has one linear region in the intermediate biases. For the MPS structure, these regions are belonging to low bias voltages ($3kT/q \le V \le 0.55$V) and intermediate bias voltage regions (0.55V ≤ V ≤ 1.30 V), respectively. Such two linear regions for MPS structure are known two parallel diodes model with different BH [31]. In addition, in the enough high forward-bias voltages, **Figure 3** plot shows for both MS and MPS structure deviation from linearity due to the existence of R_s. **Table 1**, shows the values of I_0, n and Φ_{B0} for MS and MPS structures were found from the first region as 1.90×10^{-11}A, 3.854, 0.906 eV and 7.08×10^{-10}A, 3.24, 0.80 eV, respectively. These high values of *n* for two structures at room temperature can especially be due to the existence of native or deposited interlayer, the spatially distribution of N_{ss}, and the exist of many distribution of low BHs or patches an average BH [8,14,18-20]. These results refer to the values of n and leakage current at (-6 V) for the MPS with (Zn doped-PVA) interfacial layer are lower than those of the MS attributed to the passivity role of Zn-PVA interfacial polymer layer. Similarly, the rectifying rate ($R=I_F/I_R$) at ±6V for the MPS structure is 15.5 times higher than MS structure (**Figure 3 and Table 1**).

As can be seen in eqn. (2), for MPS type structure or diode has N_{ss} in equilibrium state with semiconductor ($d_i \geq 3$ nm) and interfacial layer, the experimental results value of n becomes greater than 1 and dependent on applied bias voltage. Thus, N_{ss} can be calculated from the forward bias I-V characteristics by taking into account voltage dependent effective BH (Φ_e) and ideality factor $n(V_i)$ by using following relations [20,27,32]:

$$n\left(V_i\right) = \frac{q}{kT}\left[\frac{V_i}{ln\left(\frac{I_i}{I_0}\right)}\right] = 1 + \frac{ä}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\left(V_i\right)\right] \quad (4a)$$

$$\hat{O}_e = \hat{O}_{B0} + \hat{a}\left(V\right) = \hat{O}_{B0} + \left[1 - \frac{1}{n\left(\left(V_i\right)\right.}\right]V_i \quad (4b)$$

where β is the voltage coefficient of the effective BH used in the Φ_{B0} ($\beta = d\Phi_e/dV = 1\text{-}1/n(V)$). In calculations, the value of δ is taken as 20Å for native SiO_2 and 500 Å for (Zn-doped PVA) layer respectively. W_D is the width of the space charge region (≈3.87×10^{-5} cm which can be calculated from the linear part of reverse bias C^{-2} vs. *V* plot at 1 MHz). The value of ε_s was taken as$13.1\varepsilon_o$ for 4H SiC, the values of ε_i was taken as $3.8\varepsilon_o$ for SiO_2 and $8.47\varepsilon_o$ for Zn-doped PVA. The voltage dependent $n(V_i)$ for both structures at room temperature are obtained by using eqn. (4) and shown in

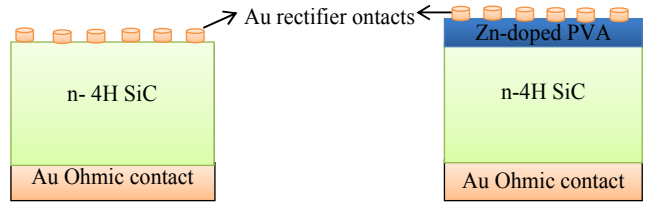

Figure 1 (a) Au/n-4H SiC (MS) structures (b) Au/(Zn-PVA)/n-4H SiC (MPS) structures.

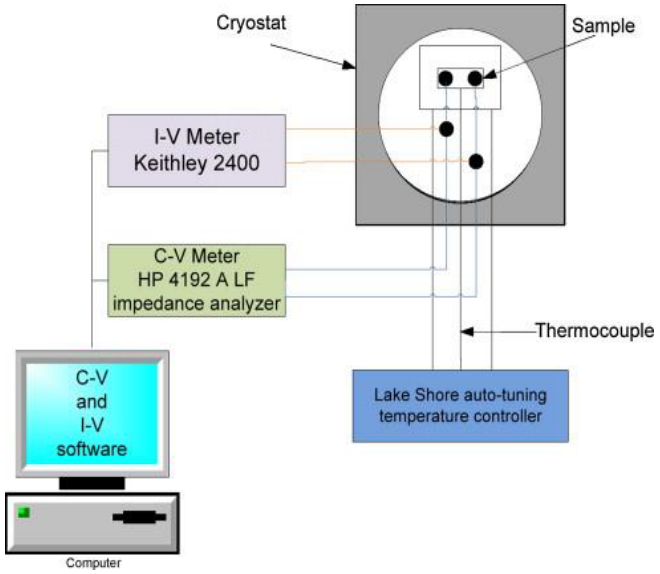

Figure 2 A simple illustration of electrical measurements system.

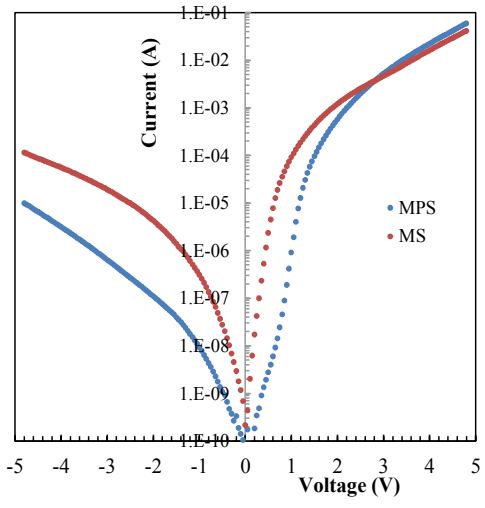

Figure 3 Experimental reverse and forward bias *I-V* characteristics for both MS and MPS type structures at room temperature.

Table 1 The experimental results values for some electrical parameters obtaind from the forward bias *I-V* characteristics for MS and MPS structure at room temperature.

Samp.	I_0 (A)	n(I-V)	Φ_{B0}(I-V) (eV)	R_s(dV/dln(I)-I) (Ω)	R_s(H(I)-I) (Ω)	RR(±6V) (=I_F/I_R)	R_s(I-V) (Ω)	R_{sh}(I-V) (Ω)
MS	2.91×10^{-11}	3.854	0.806	27.03	89.305	347	49.4	2.4×10^{7}
MPS	7.08×10^{-10}	3.241	0.815	171.72	196.79	5390	22.1	9.5×10^{8}

Figure 4. the experimental results value of n at intermediate bias voltage (for the linear region of Ln*I* vs. *V* plots) is almost constant, but it becomes increase with increasing voltage almost linearly at enough high forward bias voltages for two diodes.

In addition, the expression for the N_{ss} that is entirely governed by the semiconductor suggested by Card and Rhoderick can be simplified as follows [32].

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}\left(n(V)-1\right) - \frac{\varepsilon_s}{W_D}\right] \quad (5a)$$

The energy level of N_{ss} with respect to the bottom of the conduction band for n-type semiconductor is given by [7,21]

$$E_c - E_{ss} = q\left(\hat{\mathrm{O}}_e - V\right) \quad (5b)$$

From eqn. (4), it's clear that the value of Φ_e increases by increasing applied forward bias voltage because of the increase in quasi-Fermi energy level of majority carriers on the semiconductor side. Thus, the value of N_{ss} was calculated by using eqn. 5(a) and 5(b) and was given in **Figure 5** for both structures. As can be seen clear in **Figure 5**, the values of N_{ss} increase from the mid-gap of 4H SiC towards the bottom of conduction band (E_c). Thus the values of N_{ss} for the MPS are much lower like n and leakage current compared to the MS because of the saturation of dangling bonds or the passivity role of (Zn doped-PVA) interfacial layer. These results shows a grown of a modified PVA interfacial layer doped by Zn nanoparticles between metal and semiconductor instead of conventional SiO_2 can increases the quality and performance of the MS and MIS type structures (**Figure 5**).

Usually, the forward bias *I-V* plot for MS, MIS and MPS structures is linear on semi-logarithmic scale at intermediate forward bias voltage ($V \geq 3kT/q$), but there it becomes deviation from linear state especially because of the exist of R_s and polymeric interfacial layer. Furthermore, the experimental values of N_{ss} and resistance of the interlayer will be added to the resistance of epitaxial and so leads to deviate from linearity at enough high forward biases [17]. There are several methods to determine the value of R_s in the literature [18-20,22-24]. In this study, R_s has been calculated by applying the Cheung's method [24]. by using this method, the forward bias I-V relation with R_s value can expressed as:

$$\frac{dV}{d(lnI)} = n\frac{kT}{q} + IR_s \quad (6)$$

and

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = n\phi_B + IR_s \quad (7)$$

Both the $dV/d(\ln I)$ vs. *I* and H(*I*) vs. *I* plots were drawn by using eqns. (6) and (7) for the MS and MPS structures ant they were given in **Figures 6 and 7**, respectively. As shown in **Figures 6 and 7**, these two plots have a good linear range for two structures. Thus, a plot of dv/dln I vs. I will give the values of R_s as the slope and *n* values which determined from eqn. (6) which represent the y-axis intercept (=*nkT/q*), of these plots respectively. Similarly, the slope of H(*I*) vs. *I* plot **(Figure 7)** will provide a second way for determination of R_s, which produce a check the uniformity of this approach. From eqn. (7), the values of R_s and Φ_B were calculated and obtained from the slope and the intercept of y-axis (=$n\Phi_B$) of these plots for two structures, respectively. The values of n which are calculated from Cheung function acorrding to eqn. (6) are considerably higher than those extractes from eqn. (2). **Figure 4**, shows an expected situation due to the increase of n with applied bias voltage. The voltage dependence of structure resistance (R_i) is also obtained by applying Ohm's law ($R_i = dV_i/dI_i$) and represented inset in **Figure 3** for MS and MPS type structure. As shown in this figure, the real values of R_s and R_{sh} for both two structures agree to enough high forward bias voltage (6V) and enough low or zero bias voltages, respectively. As seen in **Table 1**, the experimental result of R_{sh} value for MPS structure is 39.99 times higher as compare with R_{sh} value for MS structure. The experimental values of R_s that obtained from Cheung's functions and Ohm's law for two structures were represented in **Table 1**. The discrepancy between R_s from these methods is the result of voltage dependence of it like ideality factor and BH.

The forward and reverse bias *C-V* and *G/ω-V* characteristics

The capacitance and conductance measurements (*C-V* and *G/ω-V*) respectively were applied at both low (1 kHz) and high (1 MHz) frequencies by using HP 4192A LF Impedance Analyzer. According to Nicollian and Brews [22], at enough low frequencies, almost of all surface states can follow the external alternating ac signal easily and so yield an excess $C_{ex.}$ and $G_{ex.}/\omega$ to the real values of them, but at high frequencies these states/traps impossible follow the ac signal. For this purpose, the *C-V* and *G/ω-V* plots of the MS and MPS structures were drawn at low frequency 1 kHz and high frequency 1 MHz. **Figure 8a and 8b** shows the *C-V* characteristics for MS and MPS structures at 1 kHz and 1 MHz, respectively, and these plots have three regions (inversion, depletion and accumulation) both low and high frequency. *C-V* characteristic has shown clearly that the anomalous peak at the accumulation region due to the effect of R_s and native SiO_2 and (Zn-doped PVA) interfacial layer rather than N_{ss}. It is clear that the magnitude of anomalous peak inversely related to frequency due to the effect of N_{ss}. This kind of peak behavior can be attributed to the particular density distribution of N_{ss} and remodeling and restructure of them under applying electric field [32-34]. As seen in **Figure 8a and 8b** the value of capacitance of both structures are extremely sensitive to the N_{ss}, interfacial layer and R_s, but N_{ss} shows an effective behavior especially at inversion and

depletion regions, whereas R_s shows an effective behavior only at accumulation region.

As seen in **Figure 8b,** at 1 MHz, C value increases with increasing voltage until accumulation region after that it suddenly decrease until goes to negative due to the effect of R_s, but at 1 kHz, this negative capacitance (NC) behavior becomes disappear. Because, the effect of R_s on C-V and G/ω-V plots can be neglected low at low frequencies, but it becomes very effective at high frequencies contrary to N_{ss}. The general consensus on NC in the accumulation region is due to the existence of N_{ss} and their relaxation time (τ), R_s, the contact injection and minority carrier injection [35,36]. In addition, according to Butcher et al. [37] and Huang et al. [38], NC behavior can be attributed to technical problems of devices, such as parasitic inductance or accuracy of calibration, respectively **(Figure 8)**.

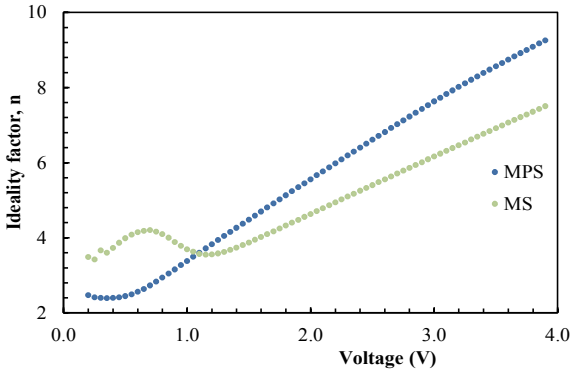

Figure 4 *n* vs. *V* for both MS and MPS structures at room temperature.

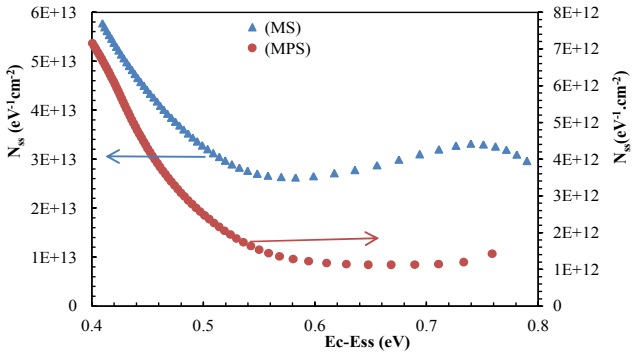

Figure 5 The energy dependent density distribution profiles of N_{ss} vs. (E_c-E_{ss}) plots for the MS and MPS structures at room temperature.

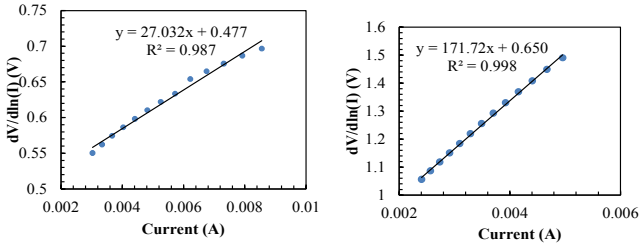

Figure 6 (a) d*V*/dln(*I*) vs. I for MS structure. (b) d*V*/dln(*I*) vs. I for MPS structure.

In general, the NC has been referred to as "abnormal" or "anomalous" behavior in the literature [33]. The C value is a differential effect of charge *Q* with respect to junction voltage V_j, i.e. $C=dQ/dV_j$ Zhu et al. [39]. Furthermore, by increasing forward bias voltage the C values reach to a maximum value and after certain voltage it started rapidly in decreasing until reach to negative value [35,39,40]. *C-V* and *G/ω-V* plots for MS and MPS structures at 1 MHz were drawn to see the inductive behavior in these structures in **Figure 9a and 9b**, respectively, which explain how the *G/ω* value increases for two structures with increasing frequency both at depletion and accumulation region, but at accumulation region contrary to *G/ω*, the value of *C* reaches a peak value and then goes to negative value at strong accumulation region. In addition, the minimum value of *C* represent the maximum value of *G/ω*. NC exhibits a decrease in electronic charges on electrodes with an increasing bias voltage and such behavior of *C* and *G/ω* is known as "inductive behavior" in the literature [33-40] **(Figure 9)**.

The variation in *C* at the reverse bias or inversion region, the C^{-2}-*V* plot of the MS and MPS structures for 1 MHz are given in **Figure 10**. As shown in **Figure 10**, the C^{-2}-*V* plot for two different type structures has a perfect linear region in the wide range of reverse bias voltage. At elevated frequencies ($f \geq$ 1MHz), the depletion layer capacitance of MS and MPS type structures can be expressed as following [18-20].

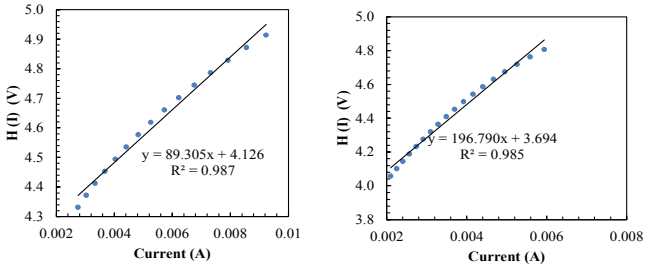

Figure 7 (a) H(*I*) vs. I for MS structure. (b) H(*I*) vs. I for MPS structure.

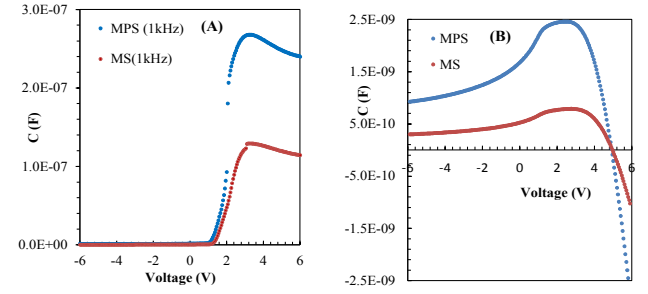

Figure 8 (a) *C-V* characteristics of MS and MPS at 1kHz (b) *C-V* characteristics of MS and MPS at 1MHz.

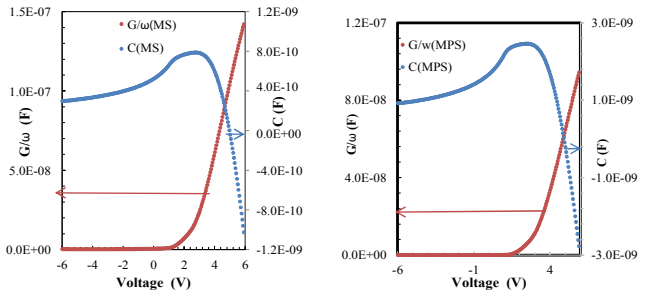

Figure 9 (a) *C-V* and *G/ω-V* plots of MS at 1MHz. (b) *C-V* and *G/ω* characteristics of MPS at 1MHz.

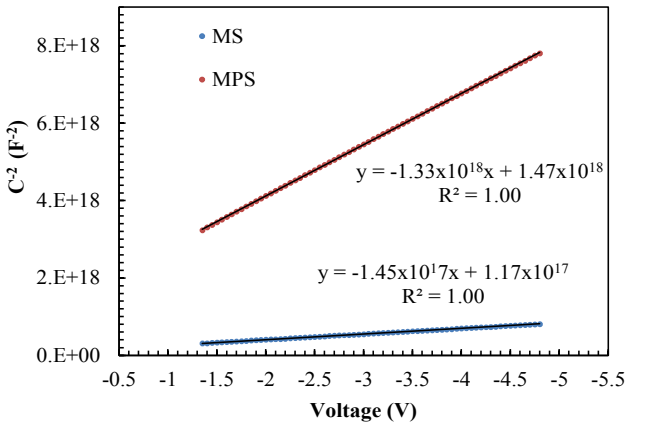

Figure 10 C^{-2} -V plots for MS and MPS structures for 1MHz at room temperature.

$$C = \frac{|dQ_{sc}|}{|dV|} = \sqrt{\frac{q\varepsilon_r\varepsilon_0 A^2 N_D}{2(V_{bi}+V)}} \text{ and } \frac{1}{C^2} = \frac{2(V_R+V_{bi})}{q\varepsilon_r\varepsilon_0 N_d A^2} \quad (8)$$

In eqn. (8), *A* represent the rectification contact area, V_R represent the reverse-bias voltage, V_{bi} represent the built-in voltage at zero bias, N_d represent the donor concentration atoms in 4H SiC, ε_r represent the permittivity of semiconductor and ε_o represent the permittivity of free space or vacuum. The values of V_o, N_d, E_F, Φ_b (*C-V*) and depletion layer width (W_D) are calculated from the intercepts and slopes of the C^2-*V* plot for each structure using following relations [18-21]:

$$V_{bi} = V_0 + \frac{kT}{q} \quad (9)$$

$$W_D = \left[\frac{2\varepsilon_r\varepsilon_0(V_R+V_{bi})}{qN_d}\right]^{\frac{1}{2}} \quad (10)$$

The value of E_F can be calculated from the conduction band edge for *n*-type semiconductor in the neutral region of n-4H SiC by using following relation as [18,19]:

$$E_F = \frac{kT}{q}\ln\left(\frac{N_c}{N_d}\right) \quad (11)$$

Where, N_c is the effective density of states in n-4H SiC conduction band. The experimental values V_o, N_d, E_F, Φ_B and W_D were obtained and arranged as in **Table 2**.

As can be seen in **Tables 1 and 2**, the Φ_{BO}(*C-V*) value which calculated from the reverse bias *C-V* characteristics is higher than Φ_{BO} (*I-V*) which calculated from the forward bias *I-V* characteristics due to the nature of measurement methods. In other words, the values of BH obtained from two techniques are not always the same in bias voltage. It is well known that the apparent BH from metal side to semiconductor side is higher than at about E_F from semiconductor to metal sides. This discrepancy between Φ_{BO} (*C-V*) and Φ_{BO} (*I-V*) is also the result of the in-homogeneities of BH and polymeric interfacial layer at M/S interface.

The profile of R_s as voltage dependent was also calculated by using eqn. (12) for the *C-V* and *G/ω* measurements by applying Nicollian and Brews method at 1MHz to explain how R_s effects on both *C-V* and *G/ω-V* characteristics for MS and MPS structure and were given in **Figure 11** [22].

$$R_s = \frac{G_{mi}}{G_{mi}^2 + (\omega C_{mi})^2} \quad (12)$$

As shown in **Figure 11**, the value of R_s at accumulation region is almost independent from applied bias voltage and so it is representing to the real value of R_s for two type structures. Thus, the real value of R_s for MS and MPS structure was found as 1.09 Ω and 1.63 Ω at 6 V, respectively. The value of R_s for MPS structure is also lower than the MS structure and these values of R_s are more suitable for an electronic device. The peak behavior in R_s vs. *V* plot for MPS structure can be caused by particular distribution of N_{ss} at (Zn doped-PVA)/n-4H SiC interface. Because, at peak position, the charge carriers may be trapped due to higher value of N_{ss} and at certain high forward biases voltage the value of R_s will decrease due to decreasing of charge carriers at traps or states. Finally, in order to see the charges at surface states or traps on the *C-V* and *G/ω-V* plots, the profiles of N_{ss} vs. *V* was also calculated from the high-low frequency (1MHz-1 kHz) capacitance (C_{HF}-C_{LF}) technique using following relation for both structures and they were given in **Figure 12**.

$$qAN_{ss} = (1/C_{LF} - 1/C_i)^{-1} - (1/C_{HF} - 1/C_i)^{-1} \quad (13)$$

In eqn. (13), C_i is the interfacial layer capacitance and was obtained by using the C_{ma} and G_{ma}/ω values at strong accumulation region at 1 MH by using following relation [22].

$$C_i = C_{ma}[1 + ((G_{ma}/\omega)/C_{ma})^2] \quad (14)$$

As seen in **Figure 12**, the density of N_{ss} for MS and MPS type structures shows a peak value due to a special density distribution of N_{ss} and their remodeling and restructure under electric field. As a result, the values of N_{ss} obtained high-low-frequency capacitance method for MPS structure are also lower than MS structure at accumulation region, but the distribution of N_{ss} varied from region to region due to their special distribution between interfacial layer and semiconductor. Furthermore,

Table 2 The expermental values of some parameters at the linear parts of the reverse bias C^{-2} vs. *V* plots for MS and MPS structure at room temperature.

Sample	V_0 (V)	N_d (cm^{-3})	E_F (eV)	Φ_B (eV)	W_D (cm)
MS	0.807	8.373×10^{16}	0.123	0.955	1.249×10^{-5}
MPS	1.105	9.128×10^{15}	0.179	1.309	3.781×10^{-5}

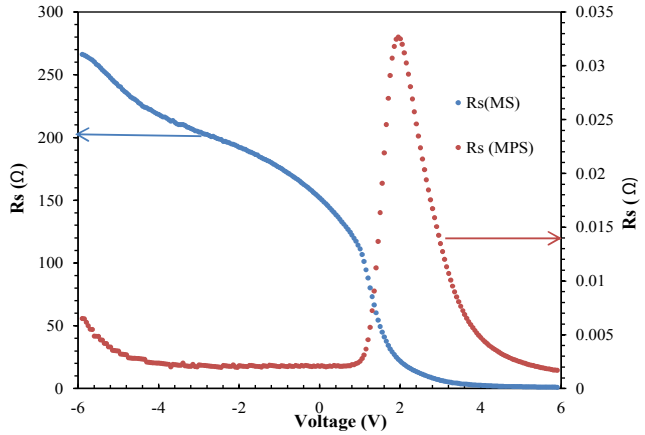

Figure 11 R_s vs. V plots of the MS and MPS structures for 1 MHz at room temperature.

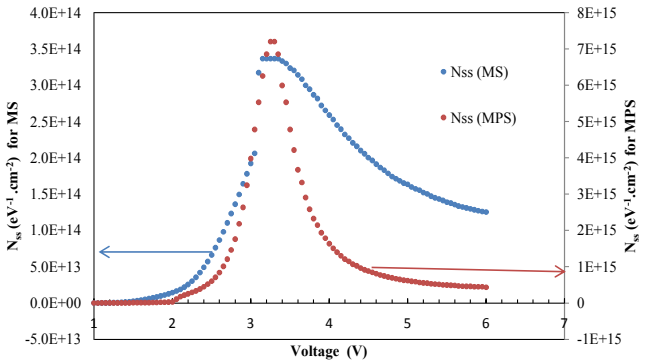

Figure 12 Profiles of N_{ss} vs. V for the MS and MPS structures obtained by the high-low frequency capacitance method at room temperature.

Figure 12 show a peak value of N_{ss} at about 3V for both MS and MPS structures with higher value for MPS 10 times than MS structure and then at higher voltage V ≥ 3 the value of N_{ss} exponentially decreases from conduction band to mid-gap with increasing applied biasing voltage in different ratio for both structures. These results indicated the electrical parameters of these structures to be quite dependent on voltage as well as interfacial polymeric layer. When the main electrical parameters of MS and MPS structure are compared; the values of ideality factor, leakage current, R_s, Φ_{Bo} and N_{ss} for MPS structure are considerably lower than the MS structure. However, the values of R_{sh} and RR for MPS structure are considerably higher than the MS structure due to the passivity role of Zn-PVA interfacial polymer layer. As a result, we can say that the (Zn doped-PVA) polymer material can be applied as an interfacial layer instead classical SiO_2 insulation layer to get better quality or performance of MS structure.

Conclusion

In this study, how the effect of modified PVA interfacial layer doped by Zn nanoparticles on the electrical parameters was evaluated and investigate after fabrication of both Au/n-4H SiC (MS) and Au/(Zn-doped PVA)/n-4H SiC (MPS) structures with the same substrate -4H SiC wafer. The main important electrical parameters are obtained from forward and reverse *I-V*, *C-V* and *G/ω-V* characteristics at room temperature to compare of them. These results show that the main electrical parameters of these MS and MPS structures are considerably dependent on voltage as well as interfacial layer.

the comparison between the two structures showing the that the higher values of BH obtained from the reverse bias *C-V* data as compare with the forward bias *I-V* data for the two structures due to the nature of the used of measurement technique. The high values of n for two structures were caused by the existence of the native and doped interfacial layer, lower barriers or patches at around mean value of BH and the existence of N_{ss} at interfacial layer/n-4H SiC interface. The profiles of N_{ss} vs. V was measured by using the forward bias *I-V* data by taking into account the voltage dependent BH and n for these two structures. The values of N_{ss} increase an exponential from the mid-gap of n-4H SiC toward the bottom of its E_c. On the other hand, the profile of R_s for these structures was measured from the *C-V* and *G/ω-V* data by applying Nicollian and Brews method. These obtained experimental results are confirmed that the effect of presence of N_{ss}, R_s, and the interfacial layer is most influential on the electrical parameters of the MS and MPS structures. In conclusion, when the main electrical parameters of both structures are compared; the values of n, leakage current, R_s, Φ_{Bo} and N_{ss} for MPS structure are lower than the MS structure, but the values of R_{sh} and RR for MPS structure are higher than the MS structure due to the passivity role of Zn-PVA interfacial polymer layer. As a result, we can say that the (Zn doped-PVA) polymer material when applied as interfacial layer instead of classical SiO_2 insulator layer, this will improve the quality or performance of MS structure.

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References

1 Reddy MSP, Kang HS, Lie JH, Reddy VR, Ja Jang S (2014 Electrical Properties and the Role of inhomogeneities at the Polyvinyl Alcohol/n-InP Schottky Barrier Interface. Appl Polym Sci 131: 139773-10.

2 Gülü Ö, Aydoğan Ş, Türüt A (2012) Electronic parameters of high barrier Au/Rhodamine-101/n-Inp Schottky diode with organic interlayer. Thin Solid Films 520: 1944-1948.

3 Altındal Yeriskin S, Balbaşı AM (2016) Tataroğlu, Frequency and voltage dependence of dielectric properties, complex electric modulus, and electrical conductivity in Au/7% graphene doped-PVA/n-Si (MPS) structures. J Appl Polym Sci 133: 43827.

4 Reddy VR (2014) Electrical properties of Au/polyvinylidene fluoride/n-InP Schottky diode with polymer interlayer. Thin Solid Films 556: 300.

5 Taşçıoğlu İ, Tüzün Özmen Ö, Sağban HM, Yağlıoğlu E, Altındal Ş (2017) Frequency Dependent Electrical and Dielectric Properties of Au/P3HT: PCBM: F4-TCNQ/n-Si Schottky Barrier Diode. J Electron Mater 46: 2379-2386.

6 Özdemir AF, Aydın SG, Aldemir DA, Görsoy SS (2011) Electrical and optical properties of p-type silicon based on polypyrrole-derivative polymer. Synth Met 161: 692-697.

7 Altındal S, Sarı B, Ünal HI, Yavas N (2009) Electrical Characteristics of Al/Polyindole Schottky Barrier Diodes. I. Temperature Dependence. J Appl Polym Sci 113: 2955-2961.

8 Bilkan Ç, Zeyrek S, San SE, Altındal Ş (2015) A compare of electrical characteristics in Al/p-Si (MS) and Al/C20H12/p-Si (MPS) type diodes using current-voltage (I-V) and capacitance-voltage (C-V) measurements. Mater Sci and Semicon Process 32: 137-144.

9 Moraki K, Bengi S, Zeyrek S, Bülbül MM, Altındal Ş (2016) Temperature dependence of characteristic parameters of the Au/C20H12/n-Si Schottky barrier diodes (SBDs) in the wide temperature range. J Mater Sci: Mater Electron 28: 3987-3996.

10 Çicek Ö, Uslu Tecimer H, Tan SO, Tecimer H, Altındal Ş, et al. (2016) Evaluation of electrical and photovoltaic behaviours as comparative of Au/n-GaAs (MS) diodes with and without pure and graphene (Gr)-doped polyvinyl alcohol (PVA) interfacial layer under dark and illuminated conditions. Composites Part B 98: 260.

11 Demir A,Yücedağ İ, Ersöz G, Altındal Ş, Baraz N, Kandaz M (2016) A Comparative Study on the Main Electrical Parameters of Au/n-Si, Au/Biphenyl-CuPc/n-Si/and Au/Biphenylsubs-CoPc/n-Si/Type Schottky Barrier Diodes. J. Nanoelectron and Optoelectron 11: 620-625.

12 Bülbül MM, Bengi S, Dökme İ, Altındal Ş, Tunç T (2010) Temperature dependent capacitance and conductance-voltage characteristics of Au/polyvinyl alcohol(Co,Zn)/n-Si Schottky diodes, J. Appl. Phys., 108: 34517-1-034517-6.

13 Altındal Ş, Uslu H (2011) The origin of anomalous peak and negative capacitance in the forward bias capacitance-voltage characteristics of Au/PVA/n-Si structures. J Appl Phys 109: 074503-1-074503-7.

14 Tunc T, Altındal Ş, Uslu I, Dökme I (2011) Temperature dependent current–voltage (I–V) characteristics of Au/n-Si (111) Schottky barrier diodes with PVA(Ni,Zn-doped) interfacial layer. Mat Sci Sem Proc 14: 139-145.

15 Gökçen M, Tunç T, Altındal Ş, Uslu İ (2012) Electrical and photocurrent characteristics of Au/PVA (Co-doped)/n-Si photoconductive diodes. Mater Sci and Eng B 177: 416-420.

16 Casady JB, Johnson RW (1996) Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review, Solid State Electron 39: 1409.

17 Sochacki M, Kolendo A, Szmidt J, Werbowy A (2005) Properties of Pt/4H-SiC Schottky diodes with interfacial layer at elevated temperatures. Solid State Electron 49: 585.

18 Sze SM (1981) Physics of Semiconductor Devices, John Wiley and Sons, Toronto.

19 Rhoderick EH (1978) Metal-Semiconductor Contacts, Oxford University Press.

20 Sharma BL (1984) Metal-semiconductor Schottky Barrier Junctions and their applications, Plenum Press, New York and London.

21 Card HC, Rhoderick EH (1971) Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes. J Phys D-Appl Phys 4: 1589-1601.

22 Nicollian EH, Brews JR (1982) MOS Physics and Technology, Wiley, New York.

23 Norde H (1979) A modified forward I-V plot for Schottky diodes with high series resistance. J Appl Phys, 50: 5052-5053.

24 Cheung SK, Cheung NV (1986) Extraction of Schottky diode parameters from forward current-voltage characteristics Appl Phys Lett 49: 85-87.

25 Tung RT (2001) Recent advances in Schottky barrier concepts. Mat Sci Engineerring 35: 1.

26 Werner JH, Guttler H (1991) Barrier inhomogeneities at Schottky contacts. J Appl Phys, 69: 1522-1533.

27 Alialy S, Altındal Ş, Tanrıkulu EE, Yıldız DE (2014) Analysis of temperature dependent current-conduction mechanisms in Au/TiO2/n-4H-SiC (metal/insulator/semiconductor) type Schottky barrier diodes. J Appl Phys, 116: 083709.

28 Kimoto T, Cooper JA (2014) Fundamentals of Silicon Carbide Technology (1.st Edn) 2014 John Wiley & Sons Singapore.

29 Kamoun O, Boukhachem A, Yumak A, Petkova P, Boubaker K, et al. (2016) Europium incorporation dynamics and some physical investigations within ZnO sprayed thin films, Materials Science in Semiconductor Processing 43: 8-16.

30 Singh PK, Gaur MS, Chauhan RS (2015) Dielectric properties of sol–gel synthesized polysulfone–ZnO nanocomposites. J Therm Anal Calorim 122: 725.

31 Demirezen, Kaya A, Vural Ö, Altındal Ş (1971) The effect of Mo-doped PVC+ TCNQ interfacial layer on the electrical properties of Au/PVC+ TCNQ/p-Si structures at room temperature, , Materials Sci. in Semicond. Proces., 33 (2015)140–148.32. H.C. Card, E.H. Rhoderick, Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes. J Phys D: Appl Phys 4: 1589.

32 Demirezen S, Kaya A, Yerişkin SA, Balbaşı M, Uslu İ (2016) Frequency and voltage dependent profile of dielectric properties, electric modulus and ac electrical conductivity in the PrBaCoO nanofiber capacitors. Results in Phys 6: 180.

33 Arslan E, Bütün S, Şafak Y, Uslu H, Taşçıoğlu İ, et al. (2011) Electrical characterization of MS and MIS structures on AlGaN/AlN/GaN heterostructures, Microelectron. Rel 51: 370.

34 Uslu H, Altındal Ş, Tunç T, Uslu İ, Mammadov TS (2011) The illumination intensity and applied bias voltage on dielectric

properties of au/polyvinyl alcohol (Co, Zn-doped)/n-Si Schottky barrier diodes, J. of Appl Polym Sci 120: 322.

35 Ershov N, Buchanan M, Wasilewski ZR, Jonscher AK (1998) Negative capacitance effect in semiconductor devices. IEEE Transactions on Electrical Devices 45: 2196.

36 Werner J, Levi AFJ, Tung RT, Anzlowar M, Pinto M (1988) Origin of the excess capacitance at intimate Schottky contacts Phys Rev Lett 60: 53-56.

37 Butcher KSA, Tansley TL, Alexiev D (1996) An instrumental solution to the phenomenon of negative capacitances in semiconductors. Solid-State Electron 39: 333-336.

38 Huang XL, Shin YG, Lim KY, Suh EH, Lee HJ, et al. (1997) Thermally induced capacitance and electric field domains in GaAs/Al0.3Ga0.7As quantum well infrared photo detector. Solid-State Electron 41: 845-850.

39 Zhu CY, Feng LF, Wang CD, Cong HX, Zhang GY, et al. (2009) Negative capacitance in light-emitting devices. Solid-State Electron 53: 324–328.

40 Bilkan Ç, Gümüş A, Altındal Ş (2015) The source of negative capacitance and anomalous peak in the forward bias capacitance-voltage in Cr/p-si Schottky barrier diodes. (SBDs) Mater Sci Semi cond Proces 39: 484-4911.