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Insights of Trap Level Effect on the Performance of InAlN/GaN High Electron Mobility Transistor (HEMT)

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Abstract

InAlN/GaN high electron mobility transistor (HEMT) structures with appropriate barrier thickness are designed to investigate the effects of trap level on the device's performance. Based on the two-dimensional drift-diffusion simulation, the influence of five trap levels of 0.3, 0.36, 0.42, 0.6 and 0.95 eV below the conduction band minimum on the DC characteristics of InAlN/GaN HEMTs are described. The results indicate that the depth of trap level obviously affects the drain current and threshold voltage of the devices, which is mainly attributed to the varied trapping rate for electrons at different trap levels according to the Shockley-Read-Hall (SRH) recombination process.

Keywords: InAlN/GaN HEMT; Barrier layer thickness; Trap level; DC characteristics

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Introduction

Over the years, as a typical representative of the third-generation wide bandgap semiconductor materials, gallium nitride (GaN) has attracted enormous attention due to its high critical electric field, polarization induced a large amount of electron gas, higher electron mobility and high saturation velocity [1,2] and the growth of AlGaN/GaN heterostructure allows to achieve high electron mobility transistors (HEMTs) with higher breakdown voltage, lower on-resistance and high operation switching frequency [3,4]. However, the AlGaN/GaN heterojunction structure suffers lattice defects due to lattice mismatch and piezoelectric effect, leading to reliability problems that have restricted the development of AlGaN/GaN heterojunction devices [5-8]. Recently, InAlN/GaN appears as a new type III-nitride heterojunction structure [9,10]. The $In_xAl_{1-x}N$ can be made lattice matched to GaN epilayer when the In composition of $In_xAl_{1-x}N$ is 0.17 [11]. The heterojunction conduction band is more discontinuous than that of AlGaN/GaN, exceeding 1 eV [11], and $In_xAl_{1-x}N$-based HEMTs exhibit higher 2DEG density thereby enabling higher drain current [12]. Moreover, $In_{0.17}Al_{0.83}N$/GaN heterostructure only produce spontaneous polarization which improves the reliability of the devices [10-13].

On the other hand, the presence of surface, bulk, or interface trap states can affect the performance of GaN-based HEMTs significantly [14]. Usually, the surface traps are considered to be factors of drain lag [15,16]. Therefore, a large amount of attention has been focused on the effects of taps on the performance of GaN-based HEMTs. Various experimental methods were employed to determine the location of traps in HEMTs, and investigated the trap-related device characteristics [17-20]. Iron-doping induced surface trap states or barrier layer trap states were explored to improve the performance of GaN-based HEMTs [21-23]. However, most of these analysis only focused on the traps on the surface or in the AlGaN barrier layer, little attention has been performed on the trapping effect in the unintentionally doped (UID) GaN buffer layers for GaN-based HEMTs. As GaN contains a high density of dislocation and various undesired complexes, impurities, and point defects, there are intrinsic trap levels in the UID GaN buffer layers. Thus, it is essential to investigate the effects of trap level in UID GaN on the performance of GaN-based HEMTs.

In this work, we firstly propose an $In_{0.17}Al_{0.83}N$/GaN HEMT structure with optimized $In_{0.17}Al_{0.83}N$ barrier thickness in terms of the threshold voltage and saturation drain current ($I_{D,max}$) based on the Silvaco TCAD simulation, and then theoretically explore the effects of different trap levels in the UID GaN buffer layer on devices' performance. As it is unclear of the exact trap level in the UID GaN buffer layer, we reasonably consider five accepter-like traps in the GaN buffer according to some experimental

studies on the location of traps in GaN [24-26], with the energy levels of 0.3, 0.36, 0.42, 0.6 and 0.95 eV, respectively, below the conduction band minimum [27,28]. The results indicate that different trap levels result in specific $I_{D,max}$ and off-state leakage current values, which is crucial for the DC characteristics of GaN-based HEMT. Furthermore, the underlying physical mechanisms of the trap level effect on the performance of $In_{0.17}Al_{0.83}N$/GaN HEMT have been explored by the recombination model and energy band analysis.

Device Description and Physical Models

Figure 1 shows the schematic diagram of the designed lattice-matched $In_{0.17}Al_{0.83}N$/GaN HEMT with asymmetric gate position. The epitaxial structure was composed of a 1 μm unintentionally dopped GaN buffer layer, with a background carrier concentration of 1×10^{16} cm^{-3} [29], and a thin layer of InAlN barrier. Ohmic contacts were formed in the source and drain terminals. The distance of gate-source, gate-drain, and length of gate were 0.5 μm, 10 μm, and 2 μm, respectively. The device surface was passivated by using Si_3N_4 thin film to reduce the current collapse effect in the HEMT [30]. It was demonstrated that the thickness of AlInN barrier layer could strongly affect the 2DEG density in the InAlN/GaN interface. Therefore, reasonable barrier thickness of 15, 20 and 25 nm were selected to optimize the HMET device structure according to experimental results [31,32], while a trap density of 5×10^{16} cm^{-3} was set in the UID GaN buffer layer.

In the calculation process, the drift-diffusion transport model was used to simulate the device response, with several important physical models of polarizations, Shockley-Read-Hall (SRH), the low field electron mobility, and high field mobility included in simulations.

Polarization modeling is critical for GaN based devices. Here, P_{PE} and P_{SP} represent the piezoelectric polarization and spontaneous polarization. The total polarization-induced polarization charge density can be expressed [33-35] as:

$$P_{total}=[P_{PE}(bottom)+P_{SP}(bottom)]-[P_{PE}(top)+P_{SP}(top)] \quad (1)$$

With

$P_{SP}(In_x AL_{1-x}N)$=-0.081+0.049x C/m²

$P_{PE}(In_x AL_{1-x}N)$=(-0.132+0.744x+0.035x²)/(3.122+0.436x) C/m²

P_{SP} (GaN)=-0.029 C/m²

The low field mobility model and high field mobility model have been used to consider various types of scattering mechanisms [32]. The low field mobility model is specified as below [34]:

$$\frac{1}{u(N,T)}=a\left(\frac{N}{1\times10^{17}}\right)\left(\frac{T}{300}\right)^{\frac{-3}{2}}\times ln\left[1+3\left(\frac{T}{300}\right)^{2}\left(\frac{N}{1\times10^{17}}\right)^{\frac{-2}{3}}\right]+b\left(\frac{T}{300}\right)^{\frac{3}{2}}+\frac{c}{\exp\left(\frac{1065}{T}\right)-1} \quad (2)$$

with a=2.61 × 10^4/$V.s.cm^{-2}$; b=9.8 × 10^{-4}/$V.cm^{-2}$ and c=1.7 × 10^{-2}/$s.m^{-2}$.

Here, $u(N,T)$ is the mobility as a function of doping and ambient temperature, N is the total doping concentration and T is the ambient temperature. The high field mobility model is described as follows [36]:

$$u(E)=\frac{u(N,T)+v_{sat}\frac{E^{(N_1-1)}}{E_c^{N_1}}}{1+a_n\left(\frac{E}{E_c}\right)^{N_2}+\left(\frac{E}{E_c}\right)^{N_1}} \quad (3)$$

where v_{sat} is saturation velocities, $u(N,T)$ is the low field mobility and E is the electric field. The values of E_c, a_n, N_1 and N_2 can be referred [36]. A trap energy level within the bandgap is caused by a structural defect in GaN. SRH recombination occurs when an electron gets trapped, referring to a trap-assisted recombination process. In order to investigate the specific physical mechanism of electron trapping, the SRH recombination model for each single trap level is required to calculate the electron trapping process. The trapping rate [36-38] is given by:

$$R_{net}^{SRH}=\frac{pn-n_{ie}^{2}}{\tau_p[n+n_{ie}exp(\frac{E_{trap}}{kT})]+\tau_n[p+n_{ie}exp(\frac{-E_{trap}}{kT})]} \quad (4)$$

where E_{trap} is the difference between the trap energy level and the intrinsic Fermi level, T is the lattice temperature, n_{ie} is intrinsic carrier concentration. τ_n and τ_p are the lifetimes of electrons and holes, respectively, both of which are assumed to be 10^{-9} S. In the formula, the electron density can be expressed as $n=N_c\exp(\frac{E_{F_n}-E_c}{kT})$ according to Fermi statistics. When only the electron trapping effect is considered, the formula can be simplified to:

$$R_{net}^{SRH}=\frac{p}{\tau_p[1+\frac{n_{ie}}{N_c\exp(\frac{E_{F_n}-E_c}{kT})}exp(\frac{E_{trap}}{kT})]} \quad (5)$$

As for the material parameters, based on LDA-1/2 approach [39], the band gap of $Al_xIn_{1-x}N$ material can be calculated by:

$$E_g^{Al_xIn_{1-x}N}=xE(AlN)+(1-x)E(InN)-bx(1-x) \quad (6)$$

with

E (ALN)=6.06 eV, E (InN)=0.95 eV, and b=3.4x+1.2

The permittivity of the material can be calculated [35] by:

$$\varepsilon_{Al_xIn_{1-x}N}=-4.3x+14.61 \quad (7)$$

$$\varepsilon_{Al_xGa_{1-x}N}=0.03x+10.28 \quad (8)$$

The relevant physical parameters of materials are listed in **Table 1.**

Results and Discussion

Figure 2 shows the direct-current (DC) characteristics of the

Table 1 Parameters of $Al_{0.83}In_{0.17}N$ and GaN sed in the simulation.

Parameter	GaN	$Al_{0.83}In_{0.17}N$
Band gap [eV]	3.42	4.62
Permittivity	10.28	11.04
Hole mobility [$v^{-1}.s^{-1}.cm^2$]	22	82
v_{sat} for electrons [10^7 $cm.s^{-1}$]	2.0	1.1

devices with three different InAlN barrier layer thicknesses of 15, 20, and 25 nm. **Figure 2a** depicts the output characteristics of the three devices with the gate voltage V_G set as 3 V, and the drain voltage V_D scanned from 0 to 35 V. It is observed that $I_{D,max}$ of the HEMTs with 15, 20, and 25 nm InAlN barrier layer are about 0.98, 1.03, and 1.08 A, respectively, indicating that the saturated drain current increases as the increase of InAlN barrier layer thickness. **Figure 2b** shows the transfer characteristics of the three devices under V_D=10 V. The threshold voltages are -1.25, -2.5, and -3.5 V for the devices with barrier thickness of 15, 20, and 25 nm, respectively, and present a negative shift as the barrier thickness increases. **Figure 2c** exhibits the effect of barrier thickness variation on the transconductance of the InAlN/GaN HEMTs. The obtained peak extrinsic transconductances are 242, 206 and 184 ms/mm at V_D=10 V for the three devices, respectively. In order to explore the dependence of the devices, DC characteristics on barrier thickness. **Figure 3** simulated the conduction band diagram of the three HEMTs at V_G=3 V. The results reveal that the depth of the electron potential well increases with the increase of barrier thickness at the InAlN/GaN interface. That would cause more electrons collection in the potential well with thicker InAlN layer, which results in the largest $I_{D,max}$ and negative threshold voltages of the device with 25 nm barrier thickness.

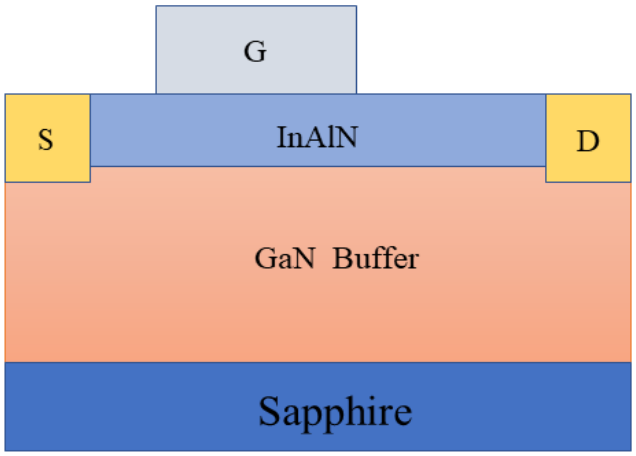

Figure 1 Schematic diagram of the designed InAlN /GaN HEMT structure.

Figure 4 shows I-V characteristics at different gate bias voltages for the InAlN/GaN HEMTs with three different barrier layer thicknesses. Can be seen that the pinch-off behavior is improved as the InAlN barrier layer thickness decreases. The cut-off phenomenon occurs at V_G=-1, -2 and -3 V for the devices with barrier thickness of 15, 20, and 25 nm, respectively, which is due to the fact that a smaller thickness of the barrier layer would cause low 2DEG density and negative threshold voltage [22], resulting in the improved pinched-off performance for HEMTs. Considering the effects of InAlN barrier thickness on both the DC and pinched-off characteristics, optimized structure of HEMT with 20 nm InAlN barrier thickness is chosen to investigate the influence of trap levels in UID GaN on the performance of InAlN/GaN HEMTs.

To explore the effects of different trap levels in the GaN buffer layer, five trap levels of 0.3, 0.36, 0.42, 0.6 and 0.95 eV below the conduction band minimum are chosen. These traps are assumed to be acceptor type traps which are unionized when V_G is below -1 V and will capture electrons when ionized. The conduction band diagrams of the HEMT structure in both the off- and on-state are simulated in **Figure 5** to investigate the distribution of carriers and further analyze the effects of different trap levels

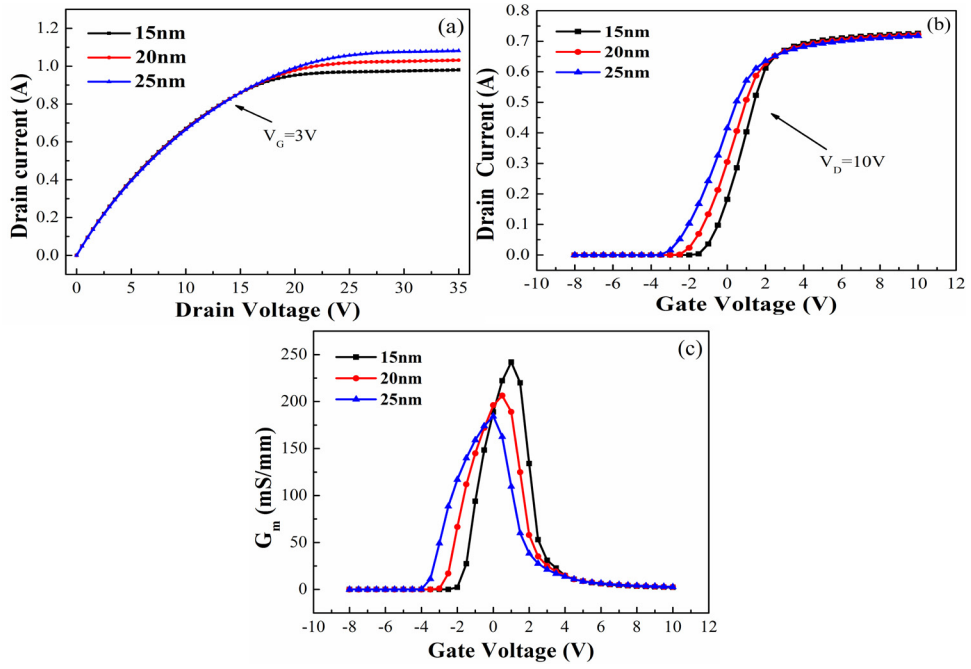

Figure 2 (a) The output characteristics, (b) transfer characteristics, and (c) transconductance of the HEMT devices with InAlN barrier thicknesses of 15, 20, and 25 nm.

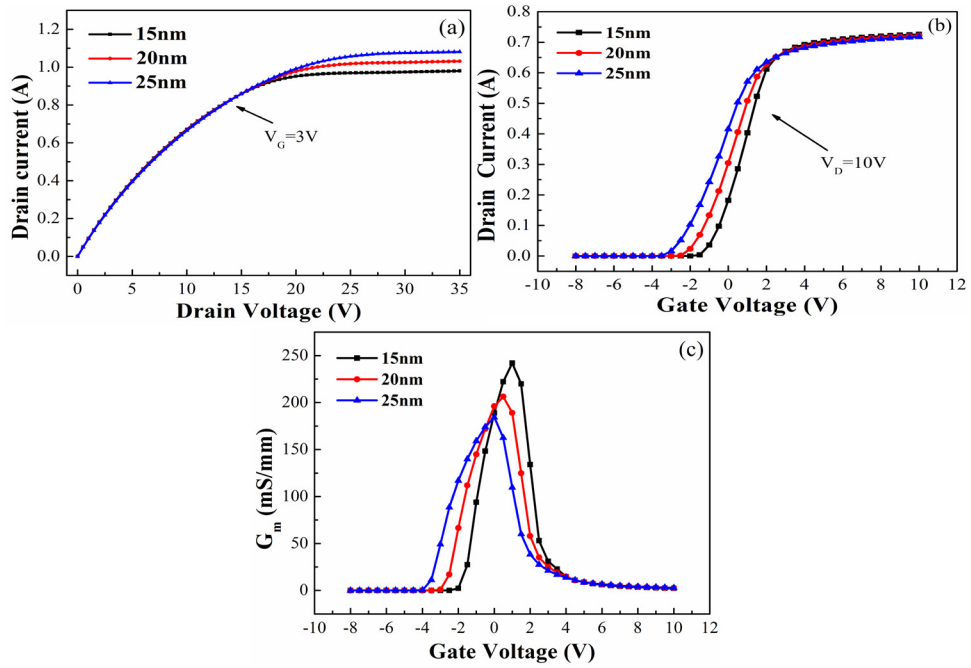

Figure 3 Conduction-band diagram of the InAlN/GaN HEMTs with different barrier thicknesses of 15, 20, and 25 nm.

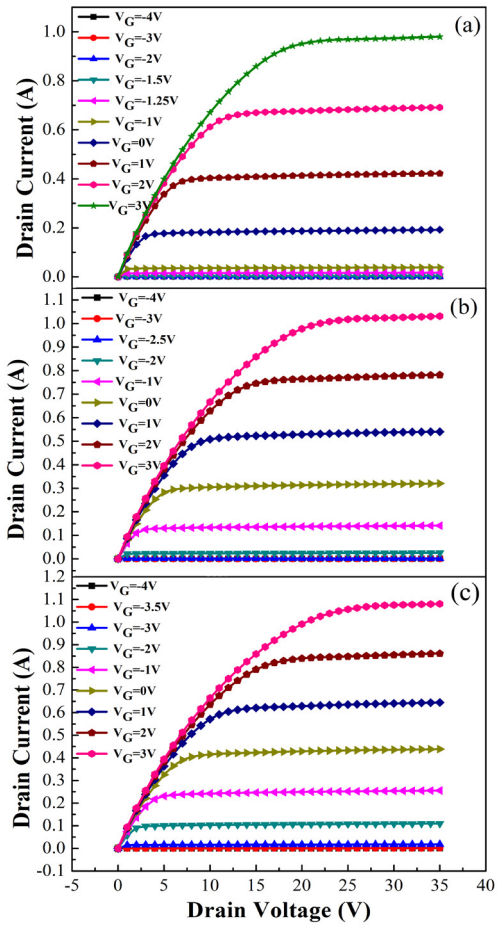

Figure 4 Simulated I-V characteristics for the HEMTs with barrier thickness of (a) 15 nm, (b) 20 nm, and (c) 25 nm as a function of gate bias voltages.

in UID GaN layer. The trap levels in the UID GaN cause changes in current that can be reflected by changes in the conduction band. As shown in **Figure 5a,** the HEMT under -5 V is pinched off, and few electrons exist at the InAlN/GaN interface. In **Figure 5b,** the HEMT under 3 V is pinched on, and the electrons would be confined in the potential well at the InAlN/GaN heterojunction interface. The depth of the electron potential well increases significantly when the device is under on-state, resulting in the variation of the $I_{D,max}$ values.

Figure 6a shows the I-V characteristics of the devices with different trap levels of 0.3, 0.36, 0.42, 0.6 and 0.95 eV in GaN buffer layer at V_G=3 V. As can be seen from the inset of **Figure 6a,** which is corresponding to the magnification of the circled area, it is evident that the five different trap levels cause different saturation currents. The $I_{D,max}$ of the device with the trap level of 0.3 eV presents the largest value of 1.02 A, while that of the device with the trap level of 0.95 eV exhibits the smallest value of 0.98 A. The saturation current as a function of the trap level is shown in **Figure 6b,** which indicates that the $I_{D,max}$ decreases as the depth of the trap level increases.

To further investigate the impacts of different trap levels in UID GaN buffer layer on $I_{D,max}$ and the distribution of carriers, the conduction band diagrams of the devices with five trap levels of E_C-0.3 eV, E_C-0.36 eV, E_C-0.42 eV, E_C-0.6 eV and E_C-0.95 eV at V_G=3 V are shown in **Figure 7a.** The electrons would be confined in the potential well at the InAlN/GaN heterojunction interface, since the InAlN/GaN HEMT is normally-on. **Figure 7b** displays the magnification of the circled area in **Figure 7a,** it is obviously seen that the height of the potential well decreases as the depth of trap level increases, which is due to the different trapping rates caused by different trap levels. According to Eq. (5), the parameter

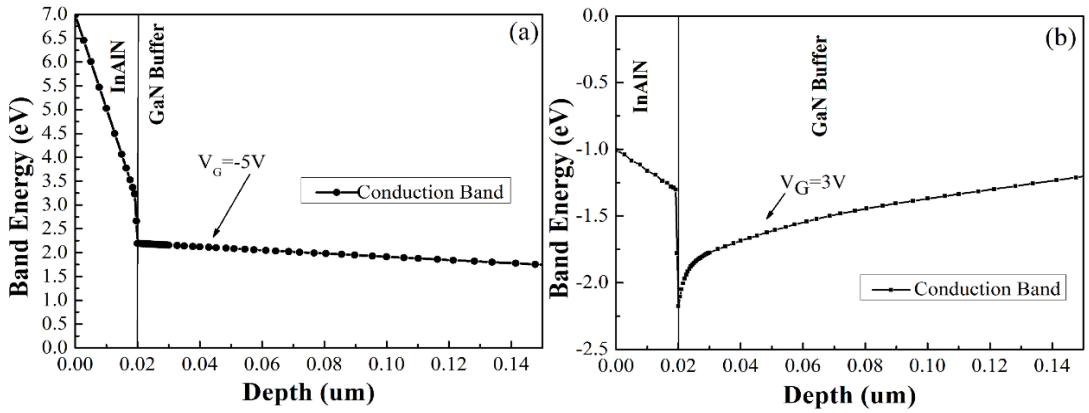

Figure 5 The conduction band diagram of InAlN/GaN HEMT at V_G=-5 V (a) and V_G=3 V (b).

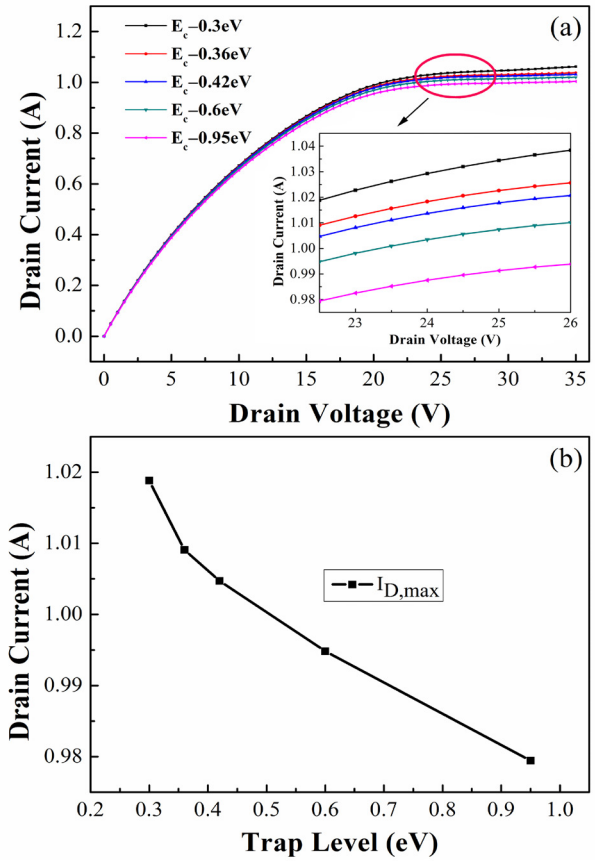

Figure 6 (a) Comparison of the output characteristics of the devices with different trap levels of 0.3, 0.36, 0.42, 0.6 and 0.95 eV in GaN buffer layer. (b) The relationship between the $I_{D,max}$ and the depth of the trap level.

R_{net}^{SRH} is effected by the value of E_{trap}, and the increase of E_{trap} can decrease the value of R_{net}^{SRH}. As E_{trap} is the difference between the trap energy level and the intrinsic Fermi level, the device with E_C-0.3 eV has the largest value of E_{trap}, while E_{trap} of the device with E_C-0.95 eV is the smallest. Therefore, the most electrons tend to be captured at the largest trap level of E_C-0.95 eV.

Figure 8a presents the transfer characteristics of the devices with different trap levels, and the enlarged region as the red circle indicated is also presented, which reveals that the threshold voltages for the five structures are almost the same of about -V. However, the off-state leakage current shows obvious variations due to different trap levels. From the relationship between the off-state leakage current and the depth of the trap level shown in **Figure 8b,** it can be seen that the trap level with the smallest depth of E_C-0.3 eV exhibits the largest off-state leakage current of 3.3 mA.

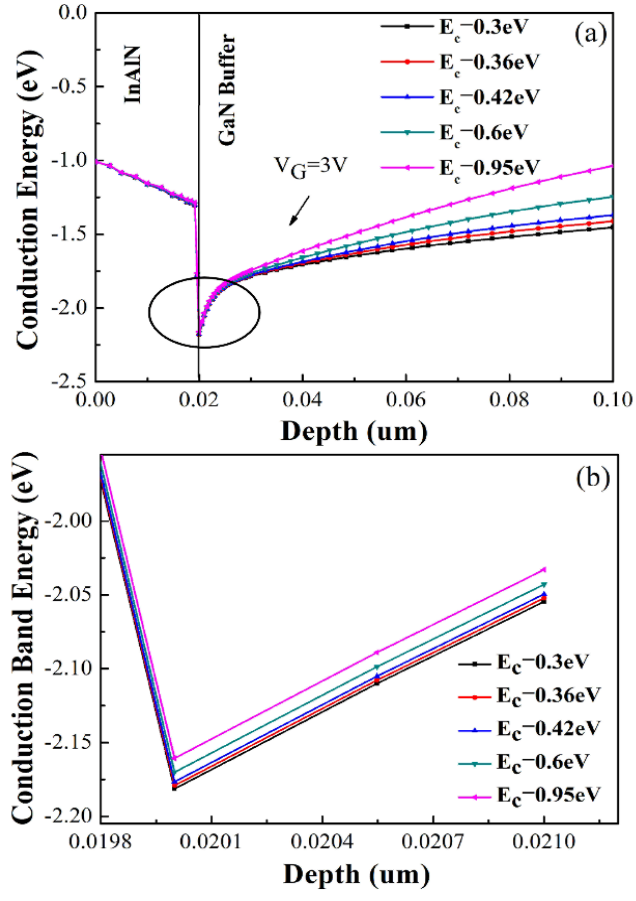

Figure 7 (a) The conduction band diagram in InAlN/GaN HEMTs with the five differnt trap levels, and (b) the enlarged band diagram as the red circle indicated.

In order to explore the effects of different trap levels in the UID GaN buffer layer on the off-state leakage current, the conduction band diagram of the devices with five trap levels of E_C-0.3 eV, E_C-0.36 eV, E_C-0.42 eV, E_C-0.6 eV and E_C-0.95 eV under pinch-off state are simulated in **Figure 9a.** It can be seen that when V_G reaches the threshold voltage (-2.5 V), the depletion layer in the InAlN layer expands to the heterojunction interface, then the 2DEG in the channel depletes and the channel is pinched off. As depicted in **Figure 9b,** corresponding to magnification of the red circled area shown in **Figure 9a,** few electrons exist at the InAlN/GaN interface when the device is under off-state. The background carriers in the UID GaN buffer layer forms a leakage channel when the HEMT is at off-state, therefore, it is necessary to introduce acceptor type traps in the forbidden band of the UID GaN buffer layer to capture electrons in the conduction band which can compensate these background electrons [40,41]. **Figure 10** obviously exhibits that the background electron concentration in the UID GaN buffer layer decreases as the trap depth increases. The background electron concentrations in the UID GaN buffer layers with trap levels of 0.3, 0.36, 0.42, 0.6, and 0.95 eV are 1×10^{12}, 1×10^{11}, 1×10^{10}, 1×10^{7}, and 1×10^{1} cm^{-3}, respectively. Based on the analysis mentioned above, the value of R_{net}^{SRH} increases as the trap level increases. Thus, more electrons are captured to compensate these background electrons as the energy level of trap increases, inducing smaller leakage current.

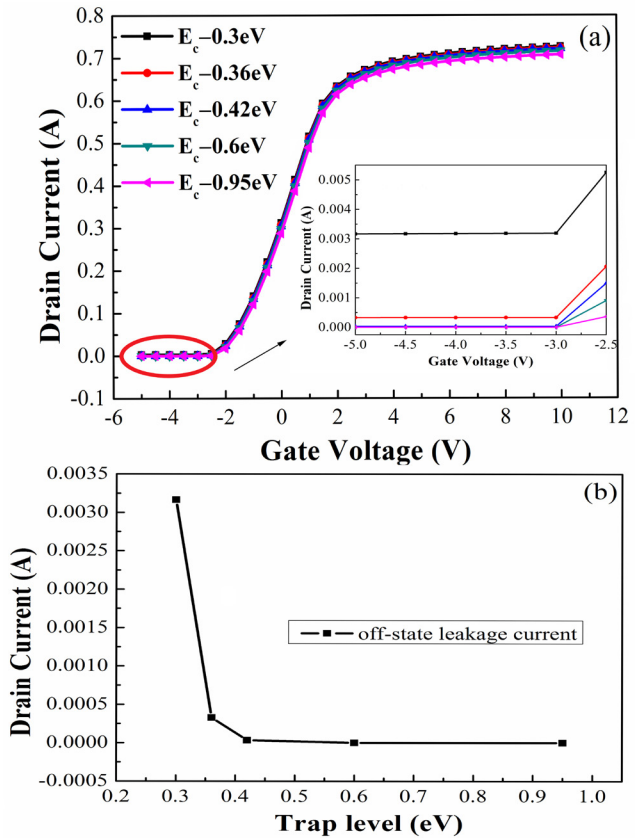

Figure 8 (a) Comparison of the transfer characteristics of the devices with different trap levels of 0.3, 0.36, 0.42, 0.6, and 0.95 eV in GaN buffer layer. (b) The relationship between the off-state leakage current and the depth of the trap level.

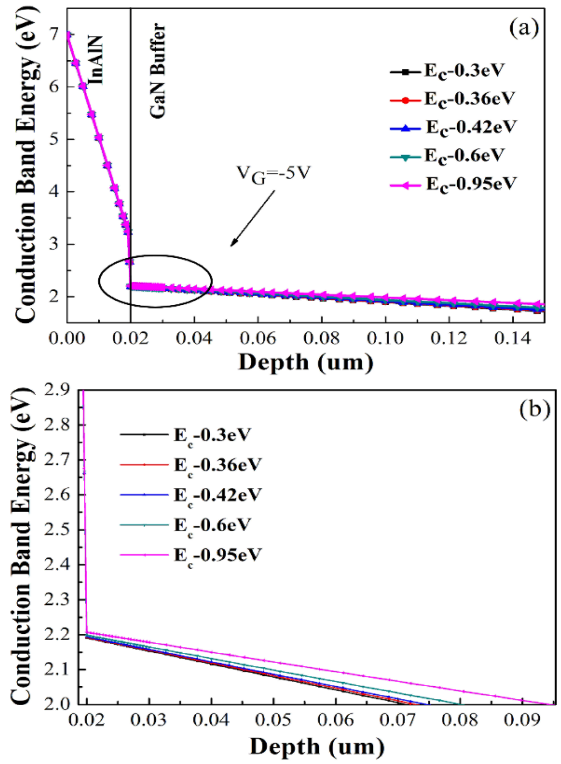

Figure 9 (a) The conduction band diagram in InAlN/GaN HEMTs with the five different trap levels. (b) The magnified band diagram as the red circle indicated.

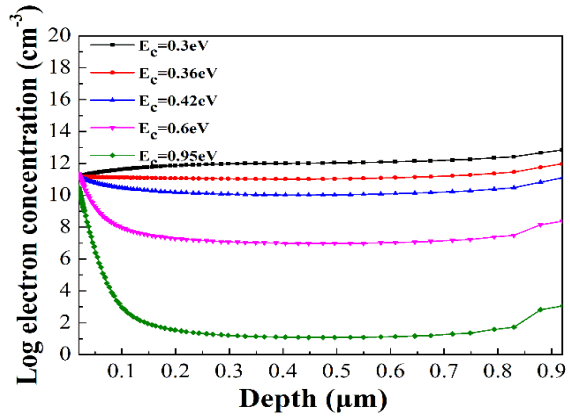

Figure 10 Electron distribution in the UID GaN buffer layer of the HEMTs with five different trap levels, when the HEMT is at off-state (applied gate voltage is -3 V).

Conclusions

In summary, a lattice-matched InAlN/GaN HEMT with appropriate barrier thickness is designed to investigate the effects of trap level in the UID GaN buffer layer on the DC performance of the devices. It is found that different depths of trap level can influence the $I_{D,max}$ and off-state leakage current of the HEMTs, which is due to that less electrons are captured from the conduction band with shallower trap level. Therefore, more electrons are collected at the InAlN/GaN interface, resulting in deeper potential well in the conduction band.

Acknowledgments

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