Available online at www.pelagiaresearchlibrary.com

Pelagia Research Library

Advances in Applied Science Research, 2011, 2 (6):190-196

ISSN: 0976-8610
CODEN (USA): AASRFC

FPGA-based Re-configurable Time Proportioning DAC

Nhivekar G. S. and Mudholkar R. R.

Department of Electronics, Shivaji University, Kolhapur, Maharashtra, India

---

ABSTRACT

In this paper we discuss the design and implementation of a simple Field Programmable Gate Array (FPGA) based time proportioning control Digital to Analog Converter (DAC) for varieties of experimental study. The paper concentrates on the Pulse Width Modulator (PWM) with time proportioning technique, which is used to convert the digital data to equivalent analog value. The results reveal the versatility of implementing dedicated circuitry.

Key words: FPGA, VHDL, PWM, Reconfigurable.

INTRODUCTION

We require a DAC (digital-to-analog converter) to interface the digital world (FPGA) to an analog one. The conventional approach would be the use of a resistor ladder or a dedicated DAC IC, like the venerable DAC-08. The simplest approach to converting digital signal to analog is to use a pulse width modulation (PWM) function together with an RC low-pass filter (LPF), as shown in Fig.1. A PWM output is just one-bit wide that generates output pulses. The pulses are made in such a way that the average value of highs and lows is proportional to the digital input. By filtering the output pulses, we obtain an analog value proportional to the digital data via PWM [1, 2]. Most common values of PWM input are 8-bits and 16-bits.An RC LPF is one of the simplest analog electronic filters that passes low frequencies well but attenuates (or reduces) the unwanted higher frequencies. By varying the duty cycle, usually controlled by a state machine or FPGA or Microcontroller, the LPF charges while the PWM signal is "on" and discharges while the PWM signal is “Off”, generating an equivalent analog output voltage corresponding to input binary data.

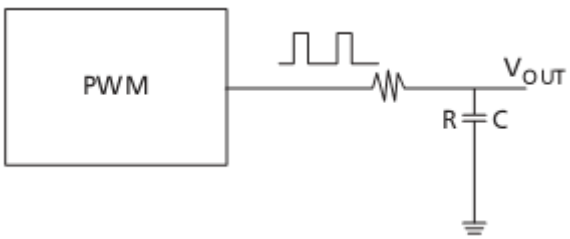

Fig.1. Model of simple DAC

This paper briefly describes the techniques of PWM control as well as design criteria for the RC filter. We are using ALTERA Cyclone-II FPGA Development Board as the hardware platform, which can be rapidly and flexibly re-configured and re-programmed by modifying its VHDL code [3]. Since the frequency at which FPGAs run is so fast compared to the frequencies required in the audio domain (MHz's compared to KHz), a one-bit DAC is a better choice in embedded applications. An FPGA-based design is perfect for producing an arbitrary-frequency generator with broad applications in biomedical devices and anywhere else that we need signals of highly accurate, precisely known frequency.

External Circuitry

To eliminate inherent noise components presented at output it is requires adding low-pass filter at output of PWM signal. Fig.2 and Fig.3 show different low-pass filter circuitries.

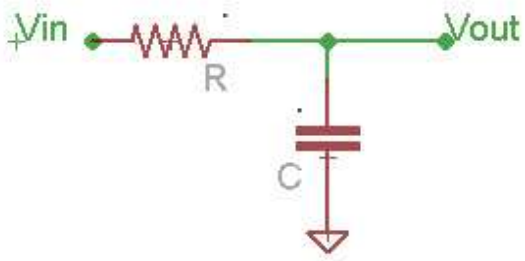

Fig. 2.First Order Passive Low-Pass Filter

First order passive low-pass filters such as those shown in Fig.2 and Fig.3 are used for low cost and low resolution requirement applications. The circuit in Fig.3 can be driven by OUTBUF and the V_{OUT} can swing from almost 0 to V_{OH} , but the V_{OUTMAX} is limited by the V_{CCI}. The circuit in Fig.2 drives a higher voltage than the devices 3.3 V limit and can be driven by TRIBUF or an open collector. Its V_{OUTMAX} can swing almost to V_{REF}, not limited by the V_{CCI}. However, R1/R2 voltage divider does not allow V_{OUTMIN} is reaching 0 V.

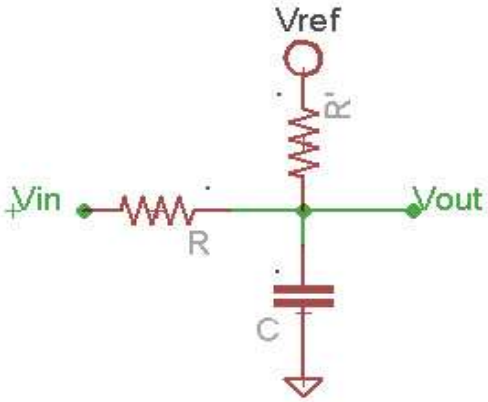

Fig.3. Modified First Order Passive Low-Pass Filter

For an application that requires $V_{OUTMAX} > V_{CCI}$, the open collector solution is desired as shown in Fig.3.

System Design Flow

Fig.4 shows a top-level schematic diagram of a typical Cyclone-II FPGA DAC implementation scheme. The inputs include Reset and Clock signals, in addition to the input binary number bus. DAC_OUT (Cyclone-II output pin) drives an external low-pass filter. V_{OUT} can be set from 0V to V_{CCO}, where V_{CCO} is the supply voltage applied to the FPGA I/O bank driving the resistor-

capacitor filter. 8-bit up/down counter counts up or down based on the PWM_in signal and generates terminal count whenever counter reaches the maximum value or when it rollback through zero. Terminal count is used to automatically load the data value to generate PWM out with different duty cycle.

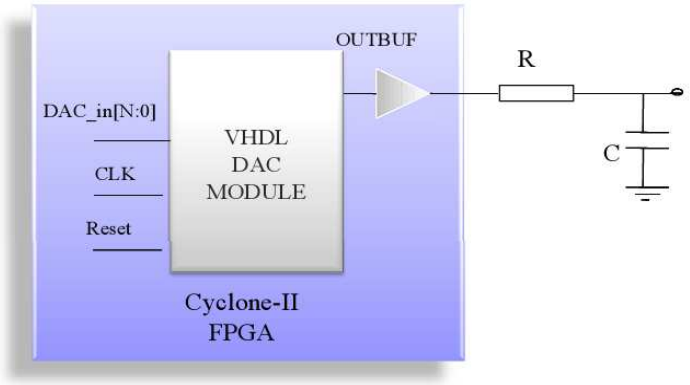

Fig.4. Top-level diagram of a typical Cyclone-II FPGA DAC

The following piece of VHDL code shows the actual behavioral description of PWM that generate the output pulse width based on input binary data (DAC_in). The design summary of program is presented in Table 1. A snapshot of the high level RTL schematic is shown in Fig.5.

```
architecture Behavioral of pwm is

begin
        PROCESS(clk)
                VARIABLE cnt_slow:INTEGER RANGE 0 TO (2147) := 0;
                VARIABLE cnt_pwm: INTEGER RANGE 0 TO (2047) := (DAC_in*8);
        BEGIN
                IF (clk'EVENT AND clk='1') THEN

                        if(cnt_pwm > 0) then
                                cnt_pwm  := cnt_pwm - 1;
                        END IF;

                        IF(cnt_slow >= CNT_SLOW_RANGE) THEN
                                cnt_pwm := DAC_in * 8;    -- LOAD pwm duty-cicle
                                cnt_slow := 0;
                        END IF;

                        IF(cnt_pwm = 0) THEN
                                out_pwm <= '0';
                        ELSE
                                out_pwm <= '1';
                        END IF;
                        cnt_slow := cnt_slow + 1;

                END IF;
        END PROCESS;
end Behavioral;
```

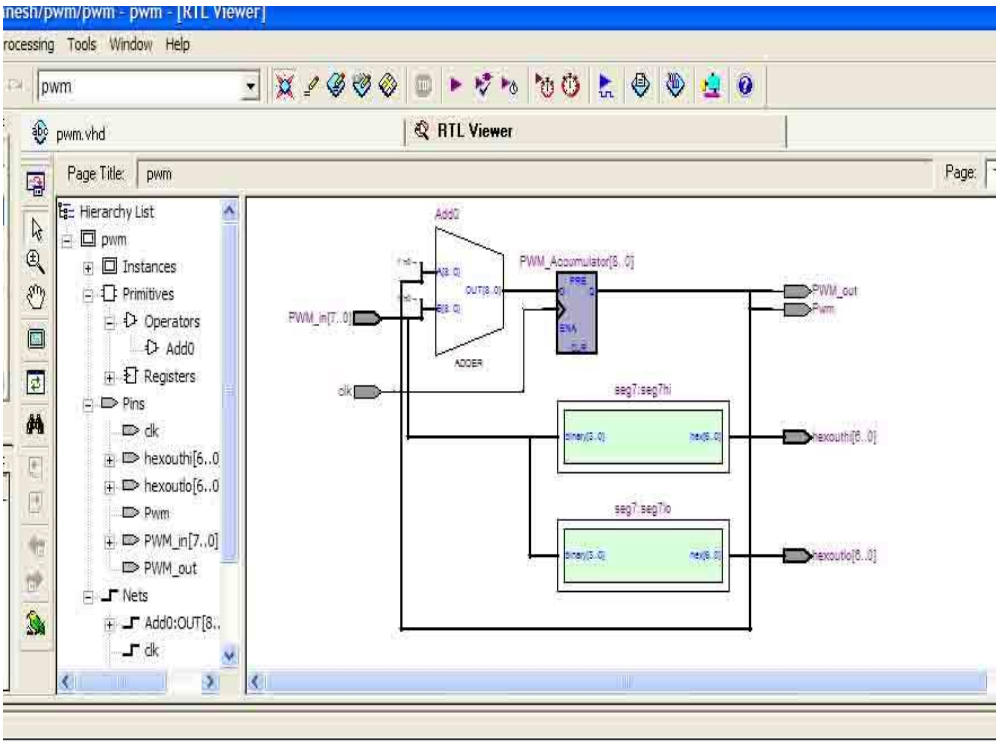

Fig.5.Top-level RTL view of a typical Cyclone-II FPGA DAC

Table 1.FPGA design summary

Top level entity name	DAC
Family	Cyclone II
Device	EP2C20F484C7
Total logic element	23
Total combinational function	23
Dedicated logic registers	9
Total registers	9
Total pin	25

BIT RESOLUTION OF PWM-DAC

The PWM counter length (L) and the smallest duty-cycle change in the PWM counter (C) determine the PWM DAC's bit resolution. The equation (1) expresses the maximum bit resolution of the PWM DAC:

For example, if the system generates an analog output voltage from a PWM DAC with a counter of 256 (L) and a minimum count step of one (C), the PWM DAC's bit resolution is 8-bits.

When the PWM resolution is determined, it is possible to calculate the Least Significant Bit (LSB) size. The LSB size is dependent upon the PWM resolution and the PWM's output-high level voltage (V_{OH}), and can be calculated using the equation (1).

$$Rbit = Log\left[\frac{L}{C}\right]\frac{\ln\left[\frac{L}{C}\right]}{\ln(2)} \qquad \ldots (1)$$

Where:
R=Resolution in Bits

L=Length of Counter (in Counts)
C=Smallest Duty Cycle Change (in Counts)
For example, in our case an 8-bit PWM DAC with a V_{OH} of 3.3V has an LSB size of 12.8mV.

RESULTS AND DISCUSSION

For translating and editing in the development environment of QUARTUS of Altera Company, the method of topmost design is adopted. That is, start at the total requirement of the system, represent the content of design hierarchy, and finally complete the whole design of the system hardware. Fig.6 gives an idea about the simulation sequence for Binary Input Data of DAC and PWM output, whereas Fig.7 demonstrates simulation sequence generated for triangular wave. From the Fig.6 and Fig.7 it is observed that how output pulse width is depend on input binary data. The simulation through ModelSim simulator validates the timing and debugging at simplicity. The VHDL modeling through the Quarts web pack presents the RTL model and gives valuable device utilization information. The photograph of FPGA-based experimental platform is shown in Fig.8.

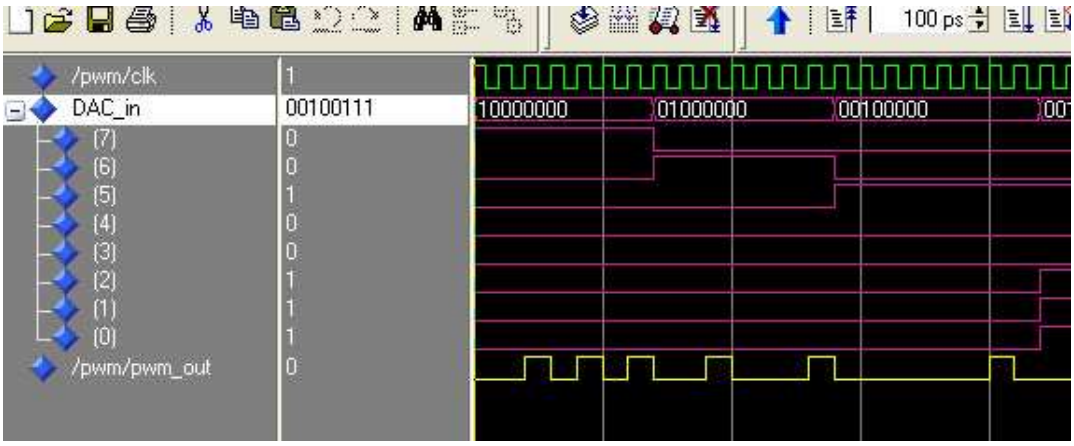

Fig.6 Simulation for Binary Input and PWM output

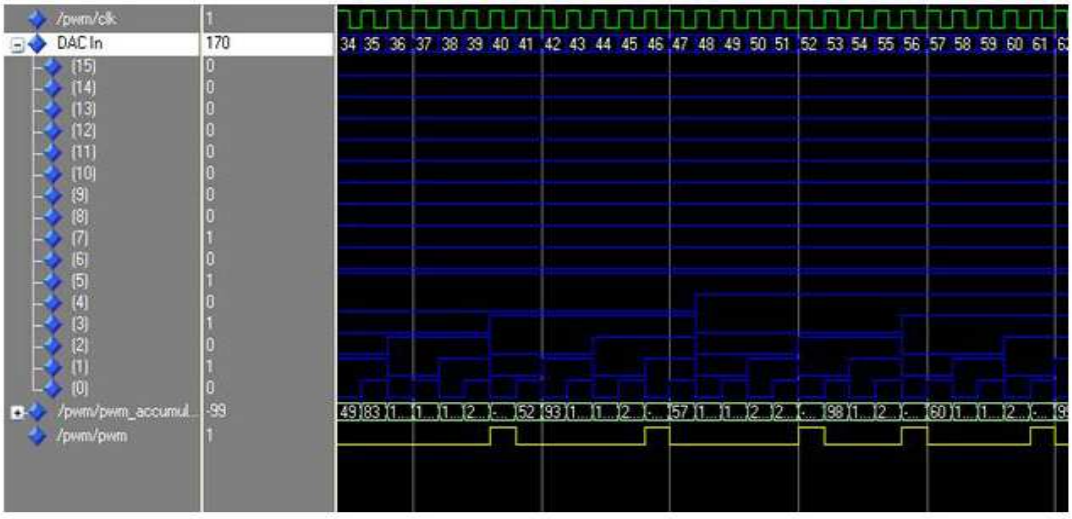

Fig.7. Simulation sequence of triangular wave

Calculated and measured output voltage of DAC is tabulated in Table 2. There is a close agreement between the calculated voltage and measured voltage and average conversion error is about 2mV.

Table 2. Observed and calculated conversion results

DAC_IN Value	Calculated Voltage(mV)	Measured Voltage(mV)	Error (mV)
0	0	1.4	-1.4
1	12.8	13.9	-1.2
3	38.4	39	-0.6
7	89.6	90	-0.4
15	192	192	0
31	396.8	395.8	1.0
63	806.4	804.3	2.4
127	1625.6	1622.8	2.8
255	3299.8	3270.0	2.9

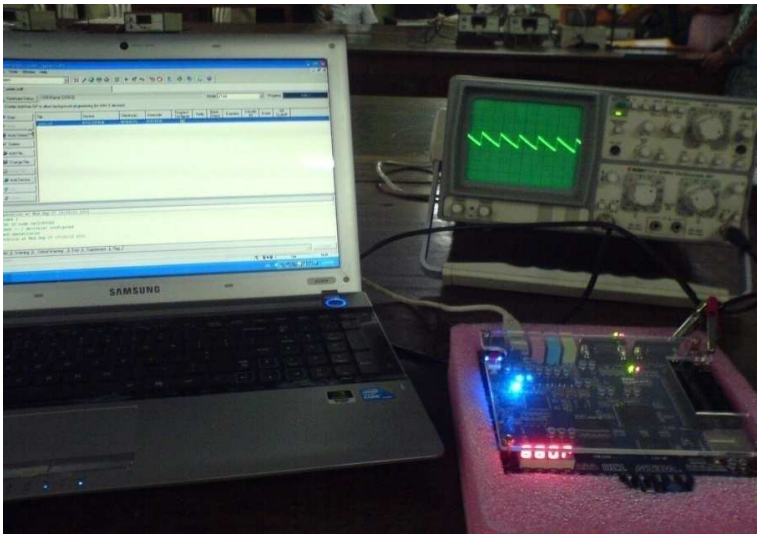

Fig.8. The FPGA-based experimental platform

CONCLUSION

The paper reports successful implementation of FPGA based time proportioning control Digital to Analog Converter (DAC) for basic experimental usage. Many embedded applications require the generation of analog signals. Although separate digital to analog converter ICs exist in the market today, synthesis of FPGA in PWM form, such as presented in this paper, can integrate these components and reduce cost and circuit board space helps to improving reliability in embedded control applications that need a PWM and low cost DAC. These techniques can be used to generate frequencies for controlling the speed of a motor, generating sound and complex waveforms, variable power supply in a power management system, programmable gain control etc. The speed and density of the Cyclone-II family of FPGAs makes them ideal for a wide range of analog signal generating and processing applications.

REFERENCES

[1]Robert McDowall, Fundamentals of HVAC Control Systems, p. 21, Elsevier Science IP Ed edition, Jun **2006**.
[2]Barr Michael, “Pulse Width Modulation” Embedded Systems Programming, September **2001**, pp. 103-104.
[3]ALTERA user guide, [online]. Available at: http://www.altera.com/

[4]Nhivekar G.S., Mudholkar R.R., *Advances in Applied Science Research*, **2011**, 2 (4),pp. 410-416
[5]Nhivekar G.S., Mudholkar R.R., *Journal of Electrical and Electronics Engineering*, **2011**, 4(1), pp.139-142.
[6]Nhivekar G.S., Mudholkar R.R., *International Journal of Engineering, Science and Technology*, **2011,** 3(4), pp. 276-283.