



Digital rate conversion with a non-rational ratio for high-speed echo-cancellation modem

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ABSTRACT

In this paper, we discuss the application of digital rate conversion in high-speed echo-cancellation modems. The requirement of rate conversion in echo-cancellation modems is first described. We then introduce the concept of digital rate conversion with a non-rational ratio and consider two types of approximations for implementation of such a rate converter. Special considerations for the application of rate conversion to echo-cancellation modems are discussed in detail. We discuss the design requirements and optimization criterion of interpolation filters for this application. The special problem of sampling clock jitter occurring in this application, its impact to modem performance and its compensation techniques are discussed.

Keywords: Digital Rate Conversion, Echo-Cancellation Modem, Non-Rational Ratio, Analogue-to-Digital Conversion, Digital-to-Analogue Conversion, Sampling, Nyquist Rate, Full-Duplex Data Transmission, DSP (Digital Signal Processor)

INTRODUCTION

To achieve efficient bi-directional data transmission over a pair of wires, called full-duplex data transmission, it is desirable to use the full available bandwidth for both transmitting and receiving at the same time. It is well known that this can be realized using echo-cancellation technology developed during the past two decades. Today, echo-cancellation is widely used in high-speed full-duplex modems.

Modern echo-cancellation modems almost exclusively use some form of Nyquist echo canceller [1] for echo-cancellation. In such an echo canceller, the received analog signal is usually first sampled at a rate higher than twice the highest frequency of the received signal. A synthesized echo is subtracted from the received signal samples. The echo-removed signal must then be re-sampled at a new rate that is synchronous to the remote transmitter symbol rate, required by the modem receiver. Classically, such a rate conversion is performed by using analog means. If analog-rate conversion is employed, two digital-to-analog converters (DACs) and two analog-to-digital converters (ADCs) must be used in the echo-cancellation modem. Due to the rapidly increased processing power and decreased cost of modern digital signal processors (DSPs), it is desirable to perform rate conversion in digital form using the available DSP. By employing digital rate conversion, the hardware parts count is reduced to one ADC and one DAC. As a result, we reduce the cost of an echo-cancellation modem and improve its reliability. It should be pointed out that the rate conversion process can be combined with echo-cancellation or equalization [2] or be implemented as a separate unit [3]. To achieve the best possible performance of the echo-canceller and equalizer, it is preferable to use a separate digital-rate converter, which we shall describe and analyze in this paper.

Digital rate conversion techniques are well known in the field of digital signal processing. While the early literature (e.g., [4,5]) had provided sound theoretical foundation for constructing such rate converters, there are many practical aspects that need to be considered and analyzed for implementation of such digital-rate converters for echo-cancellation modems. One such implementation has been described in [3]. Due to its relatively simple form, the

digital rate converter described in [3] may only be used for relatively low data bit rates. The performance and design of digital rate converters to be used in high-speed echo-cancellation modems, represented by the CCLTT recommendation V.32 bis and the proposed V. fast recommendation, must be carefully analyzed for optimization of its performance, stability and complexity. These important aspects of application of digital rate conversion techniques to echo-cancellation modems are the subjects of this paper. This paper is organized as follows:

In Section 2, we discuss why rate conversion is needed and how it is used in echo-cancellation modems. Classical analog implementations of rate conversion in echo-cancellation modems are described. The principle of digital rate conversion is the topic of Section 3. The application and implementation considerations of digital interpolation to perform rate conversion with a non-rational ratio in echo-cancellation modems are then described in detail in Section 4. In Section 5, we discuss compensation of sampling clock jitter. This is a special problem occurring in such an application that affects the performance and stability of echo-cancellation modems with digital rate conversion. Section 6 concludes this paper.

SAMPLING RATE CONVERSION IN ECHO-CANCELLATION MODEMS

In an echo-cancellation modem employing a real Nyquist echo canceller, the received signal, called RX signal in the sequel, from the receiving port of its hybrid coupler is sampled at a rate that is higher than twice the highest frequency component in the signal, i.e., its Nyquist rate. The RX signal samples contain both the signal from the remote modem and the echo of the local transmitted signal. To perform effective echo cancellation, it is desirable to let the sampling rate be equal to an integer multiple of the modem's transmitting symbol rate, called the local TX symbol rate, denoted as $1/T_{TX}$. We express the sampling rate by m/T_{TX} , where m is an integer. Synthesized echo samples, usually also at m/T_{TX} , are constructed from the TX digital symbols and subtracted from the RX signal samples. The echo subtraction can be implemented either in analog form or digitally, and the signal at the subtractor output would be almost echo-free. The echo-removed RX signal is sent to the equalizer of the modem to recover the remotely transmitted data. To effectively perform equalization, it is desirable that the RX samples received by the equalizer is at a rate that is an integer multiple of the remote transmitter symbol rate denoted as $1/T_{RX}$. It is usually convenient to let the RX sampling rate equal m/T_{RX} . Nominally, T_{TX} and T_{RX} are equal to each other in almost all echo-cancellation modems. However, they are practically never exactly the same. Thus, it is necessary to convert the rate of the RX samples from m/T_{TX} to m/T_{RX} after echo-cancellation. A block diagram of an echo-cancellation modem is depicted in Figure 1. Further details of the principle and operation of echo-cancellation modems can be found in [7] and [8].

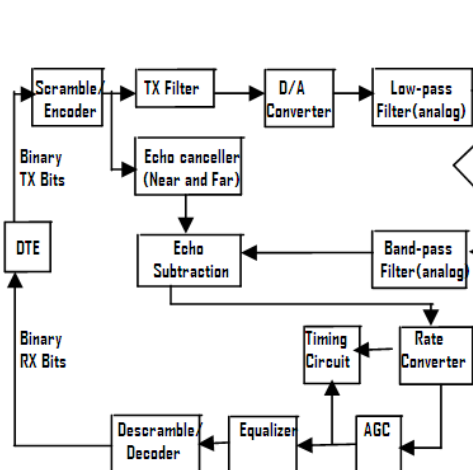


Fig. 1: Block Diagram of an Echo-Cancellation Modem

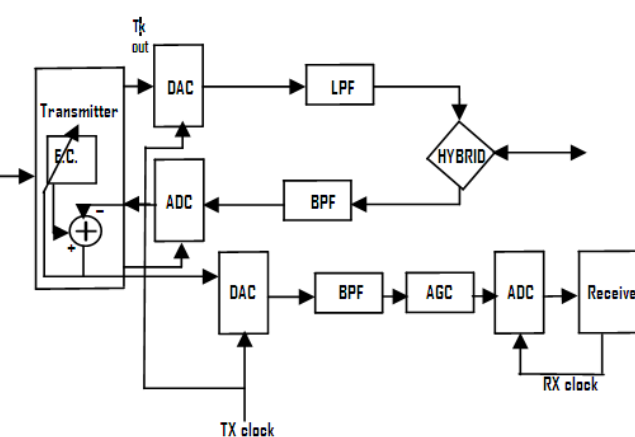


Fig. 2: An Echo-cancellation Modem with Digital-Subtraction/Analog-Rate-Conversion

Rate conversion can be realized by using either analog or digital means. Classically, analog rate converters are commonly used. Two arrangements of echo subtraction and analog rate conversion techniques are described below. Figure 2 shows the block diagram for performing analog subtraction and analog rate conversion. The synthesized echo samples at frequency m/T_{TX} is converted to analog form by using a DAC and holding that value for one sample time interval. The received signal is also sampled at the same rate and the analog samples also held for one sample interval. These sampled/held analog values are applied to an analog subtractor, which is usually realized using a conventional operational amplifier. After the input values are stabilized, the difference (error) signal at the subtractor output is then converted to digital values using an analog-to-digital converter (ADC). The digital error signals are used by the echo canceller for updating its coefficients. At the same time, the subtractor output also passes through a low-pass analog filter to remove its high frequency components. The filtered analog signal is then sampled by

another ADC, which is controlled by a timing recovery circuit that recovers the remote clock, at a rate synchronous to the remote transmitter clock, i.e., m/T_{RX} .

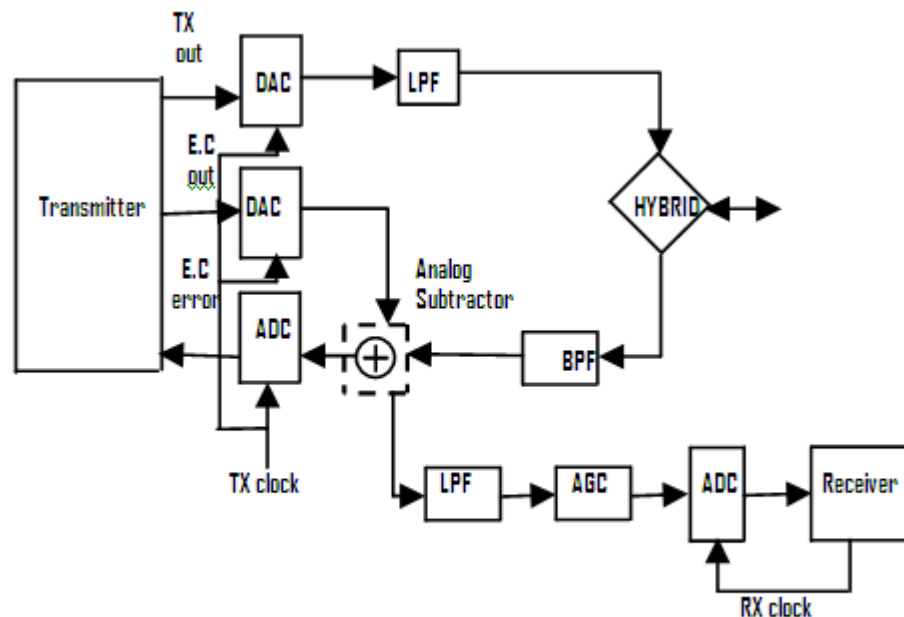


Fig. 3: An Echo-Cancellation Modem with Analog-Subtraction/Analog-Rate-Conversion

Figure 3 shows an arrangement using digital echo subtraction. The received signal is first converted to digital samples by a first ADC at frequency m/T_{TX} . The digital synthesized echo, which is also at m/T_{TX} , is subtracted from the digital received signal samples. The difference (error) digital samples are directly used to update echo canceller coefficients. The digital error signal is also sent to a DAC to be converted to analog form. The converted analog error signal, which is in a staircase form, passes through an analog low-pass filter. The filtered analog signal is then converted to digital form to be used by the receiver as described above.

Comparing the above two schemes, we note that a modem with either implementation needs two ADCs and two DACs (including the one in the transmitter). The difference is that the ADC's of the first scheme require less precision.

It can be seen from the above description that, in either of analog rate conversion schemes, a pair of ADC/DAC are needed for converting a digital signal from one rate to another. It is well known that the digital samples of an analog signal contain all the original information of the analog signal as long as the sampling rate is above the Nyquist rate of the analog signal. Thus, it is possible to convert a digital sample sequence at a first sampling rate to a new digital sample sequence at another rate using only digital signal processing techniques. Such digital rate conversion techniques have been discussed in the literature. Please refer to [4], [5] and [6] for better understanding of digital rate conversion. Below we summarize the basic principles useful for the application in echo-cancellation modems.

DIGITAL RATE CONVERSION

In principle, a digital rate converter can be implemented using a 1:N digital interpolator that consists of a bank of N finite impulse response (FIR) subfilters. Each of the subfilters has the same ideal low-pass magnitude response but a different group delay, which differs by a fixed small amount from one to another within its passband. By selecting the proper subfilter for generating each output sample, we can generate an output sample sequence that has the same frequency spectrum as the input sequence but is sampled at different and arbitrary sampling time instances, also called timing phases. As a result, we can realize rate conversion at an arbitrary rational ratio, provided the number N of the subfilters is large enough. However, increasing the number of subfilters means increasing the required memory storage. Moreover, as can be seen from the discussion given in Section 2, for rate conversion in echo-cancellation modems, the conversion ratio may be a non-rational number, which is not exactly known and is likely to change with time. Thus, exact rate conversion is neither practical nor possible.

Practically, a small error always exists in the conversion process due to the imperfection of the interpolation filter. Furthermore, a small error will not impair the modem performance as long as it is far below the noise level allowed

by the receiver. Thus, to generate a certain output sample, we can use the subfilter that has the delay closest to the desired delay of the sample. For example, N may be chosen in the range between 16 and 1024. To reduce the number of subfilters, while improving the accuracy of rate conversion, we can interpolate the outputs of two adjacent subfilters to obtain one output sample such that the desired delay is between the delays of these two interpolation filter output samples. The desired output can be computed using linear interpolation of the samples. It can be shown that by using linear interpolation, letting N be a small number suffices for rate conversion in echo-cancellation modems. The cost paid is that we double the required computation because two interpolation filter output samples need to be computed to generate one output sample. How much error introduced by the interpolation process that can be tolerated depends on the particular application. For high-speed echo-cancellation modems, a signal-to-noise ratio (SNR) of 30 to 40 dB is generally required by the receiver. The error introduced by the interpolation filter should be far below the required SNR.

A detailed analysis on the relationship between the mean squared error due to the approximation in digital interpolation and the number of coefficients can be found in [6]. Below, we only state the conclusions.

It can be shown that without linear interpolation, the normalized mean squared error (MSE) ρ_e is bounded by

$$\rho_e \leq \frac{\omega_h^2}{12N^2}$$

where ω_h is the normalized highest received signal frequency (in radians/second) and N is the number of interpolation filters. On the other hand, when linear interpolation is used, we have

$$\rho_e \leq \frac{\omega_h^4}{80N^4}$$

As is shown in [6], if $\omega_h = 0.8\pi$, and the required $\rho_e < -50$ dB, we require $N = 230$ and $N = 15$, for digital rate conversion without and with linear interpolation, respectively. It is obvious from this example that when the SNR requirement is high, using linear interpolation can greatly reduce the required number of interpolation filter coefficients.

ECHO-CANCELLATION MODEMS WITH DIGITAL RATE CONVERSION

Figure 4 shows a block diagram of an echo-cancellation modem using digital-echo-subtraction/digital-rate-conversion. The echo subtraction operation is the same as the digital-subtraction/analog-rate-conversion method described above. After the digital error samples are generated, they are fed to a digital rate converter described above. The digital rate converter is controlled by a timing recovery circuit, which consists of a timing-error detector and a digital phase-locked loop (DPLL). The principles of the timing-error detector and the DPLL are well documented in the literature such as [7]. The timing-error detector detects sample-timing phase error between the digital rate converter output samples and the remote transmitter clock whose information is embedded in the received signal samples. The output of the DPLL represents the timing-phase difference between the remote TX clock and the digital rate converter output sample. If the output sampling frequency is lower than the input sampling frequency, the offset gradually increases. Its desired sampling time is moving towards the sampling time of the next input sample. Once the sampling time of the input and output samples become the same again, the offset becomes zero again. The sampling time offset is realized by using different subfilters, linear interpolation and properly shifting the samples in the delay line of the interpolation filter.

It can be seen that the phase detector, the DPLL and the rate converter form a negative feedback loop. After the start-up period, the timing phase-error detector output should become zero on average. As a result, the output samples of the digital rate converter are synchronous to the remote TX clock and are used by the equalizer for recovering the remotely transmitted data. In most cases, the local and the remote TX symbol rates are nominally equal to each other. Thus, the conversion rate can be chosen to be close to one. In such a case, the interpolation filter is totally controlled by the DPLL. For asymmetric transmitting and receiving rates, we need to add a fixed offset to the DPLL output each time when an output sample is generated.

It should be noted that, since the rate converter is always followed by an equalizer, the criterion of designing the optimal interpolation filter is different from that for conventional digital rate converters. Conventionally, we would like to design an interpolation filter which approximately has an overall ideal lowpass frequency response, i.e., it is close to a constant over the passband. For our application, it is more important that the subfilters have the magnitude responses as similar to each other as possible. The magnitude is not necessary to be a constant within the passband as long as the equalizer can compensate the overall response including the TX filter, the channel, and the interpolation filter. The delay responses of the subfilters should still differ by a constant of $1/NT_{TX}$ over the entire passband from each other.

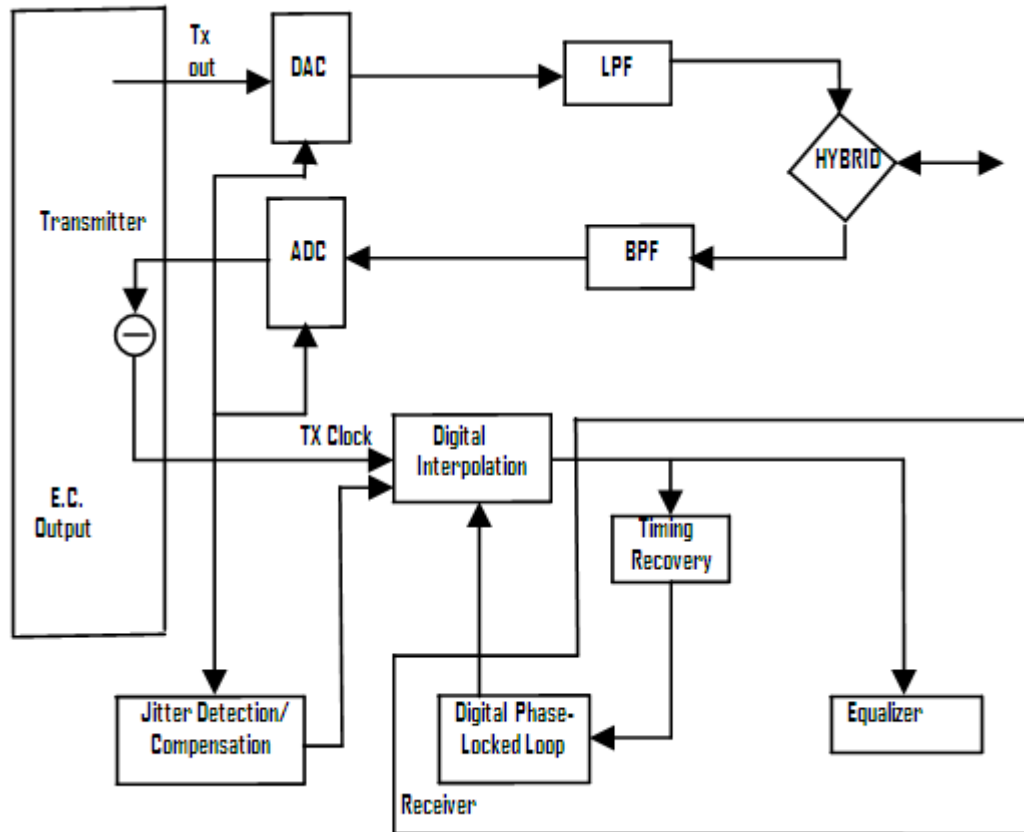


Fig. 4: An Echo-Cancellation Modem with Digital-Subtraction/Digital-Rate-Conversion

In Figure 4, we have also shown a jitter compensation circuit which is necessary to ensure the proper operation and the stability of the modem, as discussed below.

COMPENSATION OF JITTER IN SAMPLING CLOCK

Since the digital rate conversion uses the input data sequence as a reference, it is only accurate when the input samples are generated by a stable clock. For conventional digital rate conversion, it is usually true that the sampling clock is indeed a stable clock, such as one generated by a crystal oscillator. However, in the application considered here, the ADC that generates input sample is governed by the local TX clock. This clock may be jittery when the modem is in external timing mode loop-back timing mode for synchronous data transmission. When the input sampling clock is not stable, jitter of the input sampling clock will cause jitter at the output samples. Such jitter degrades the performance of the modem and may even cause instability of modem operation in the loop-back timing mode. To improve modem performance and stabilize its operation, such jitter must be compensated.

To compensate the sampling clock jitter, we need to measure the magnitude of the jitter. The result is then used to compensate for the jitter in the rate converter.

It has been shown in practice that the compensation technique greatly reduces the jitter in the samples sent to the equalizer and improves the modem performance in external timing mode and loop-back timing mode. It also solves the potential stability problem in loop-back timing mode. However, it should be pointed out that the compensation will never be perfect and there may exist a small residual timing error, which will eventually accumulate to affect normal modem operation. This timing error may also be caused by numerical inaccuracy in computation of the rate conversion. Some safeguard measures must be taken to prevent long-term drifting for ensuring normal operation of the echo-cancellation modem.

Furthermore, we would like to point out that the problems dealt with in this section are important mainly for high-speed echo-cancellation modems operated in synchronous mode. If we are interested in a relatively low-speed asynchronous modem, e.g., a 9600 bps V.32 modem in asynchronous mode, these problems may become insignificant or can be solved using other simpler methods.

CONCLUSION

In this paper, we discussed the application of digital rate conversion in echo-cancellation modems. Due to the nature of the application, the conversion ratio is not a predetermined or fixed rational number. Thus, we introduced the concept of digital rate conversion with a non-rational ratio and considered the approximate implementations of such a rate converter. Two types of approximations: using a large number of filter banks and using linear interpolation in conjunction with a much smaller set of interpolation filter bank were considered. It is shown that linear interpolation may become necessary if high signal-to-noise ratio is required by the receiver for V.32 bis and V. fast echo-cancellation modems.

While the concept of digital rate conversion is well known in the field of multirate digital signal processing, special considerations must be taken into account for its applications to echo-cancellation modems. In this paper, we discussed the design requirements and optimization criterion of interpolation filters for this application. The special problem of sampling clock jitter occurring from this application and its compensation were also discussed.

Digital rate conversion has been successfully implemented in high-speed echo-cancellation modems at data rates up to 28.8 kbps. Due to the increasingly widespread applications of high-speed digital signal processors, more and more signal processing tasks previously realized using analog components are now being implemented using digital signal processing techniques. We expect that digital rate conversion will find more and more usage in various DSP applications.

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