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Characteristics and stability of GAAS thin film transistors

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ABSTRACT

GaAs, a promising candidate for optoelectronic devices has been used in Thin Film Transistors (TFTs) with a rare earth oxide (Nd_2O_3) as gate insulator. The samples are fabricated in staggered electrode structure by multiple pump down (MPD) method of vacuum evaporation. The device parameters have been evaluated from the characteristics and suitable theoretical model. Stability is assessed through periodic observation of the characteristics. The TFTs exhibited good channel modulation but poor stability and were sensitive to humidity.

Key words: Thin Film Transistors, device characteristics, stability.

INTRODUCTION

Thin Film Transistors are of current interest for their suitability in large area circuits. Poly silicon and amorphous Si thin films are successfully used in TFTs. But little attention has been paid to GaAs which is also a candidate material for optoelectronic devices like solar cells and sensors [1]. Though investigation on GaAs for high speed devices and microwave applications has been accelerated in recent years its use in TFTs is rare in the literature. The performance of an active device depends primarily on the physical properties of the materials used in its fabrication [2]. Again the stability of any TFT is principally a function of gate insulator properties [3]. A poor quality dielectric can increase the leakage current [4]. The insulator film should be stoichiometric with minimum incomplete bonds and free from pores which are colourless and transparent [5]. Out of all rare earth oxides Nd_2O_3 is reported to be the most suitable as gate insulator in TFTs [6]. Vacuum evaporated Nd_2O_3 films having chemical and mechanical stability, high breakdown field strength (1.5 x 10^6 V cm^{-1}), low dissipation factor (~.0045) and high dielectric constant (12.64) fulfills the requirements of good insulators [7]. As such TFTs with a new semiconductor-insulator combination is investigated and their characteristics are presented in this paper.

MATERIALS AND METHODS

TFTs have been fabricated by MPD method on chemically and ultrasonically cleaned glass substrates by vacuum deposition of different layers in the given sequence: aluminium source drain electrode, GaAs film at elevated substrate temperature (200°C), Nd_2O_3 layer as gate insulator and finally the aluminium gate electrode. Various geometrical patterns were obtained with the help of mechanical masks. The channel was defined by a 50 µm wire grill fixed on the source drain mask. All the depositions were made in vacuum of the order of 10^{-6} torr. Film thickness was measured by multiple beam interference method. The fabricated samples were annealed in air at 200 °C for 3-4 hours and then stored in clean desiccator for 20-25 days to obtain stable and saturated characteristics. To assess the impact of ambient atmosphere the stability of the devices I-V data was recorded at different periods of time. Thereafter the samples were left in ambient atmosphere and I-V data was noted till the TFTs collapsed. Some important transistor parameters like trans conductance and mobility were also evaluated from time to time.

RESULTS AND DISCUSSION

The source-drain characteristics of a fresh sample of GaAs - Nd_2O_3 TFT at different gate voltages (V_G) are shown in figure 1. Figure 2 shows the characteristics of the fresh sample (curve 'a'), after 30 days (curve 'b'), 45days (curve 'c') and 60 days (curve'd') in clean desiccators. While the curves 'e' and 'f' are the characteristics of the sample in ambient atmosphere after 15 days and 30 days respectively at $V_G = -5V$.

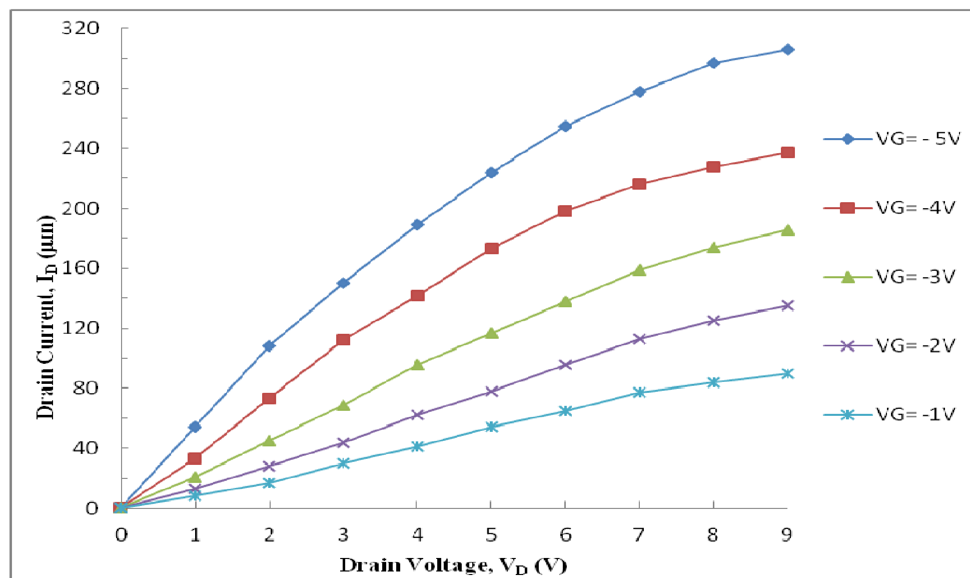

Figure1: Source- drain characteristics of a fresh sample of GaAs - Nd_2O_3 TFT.

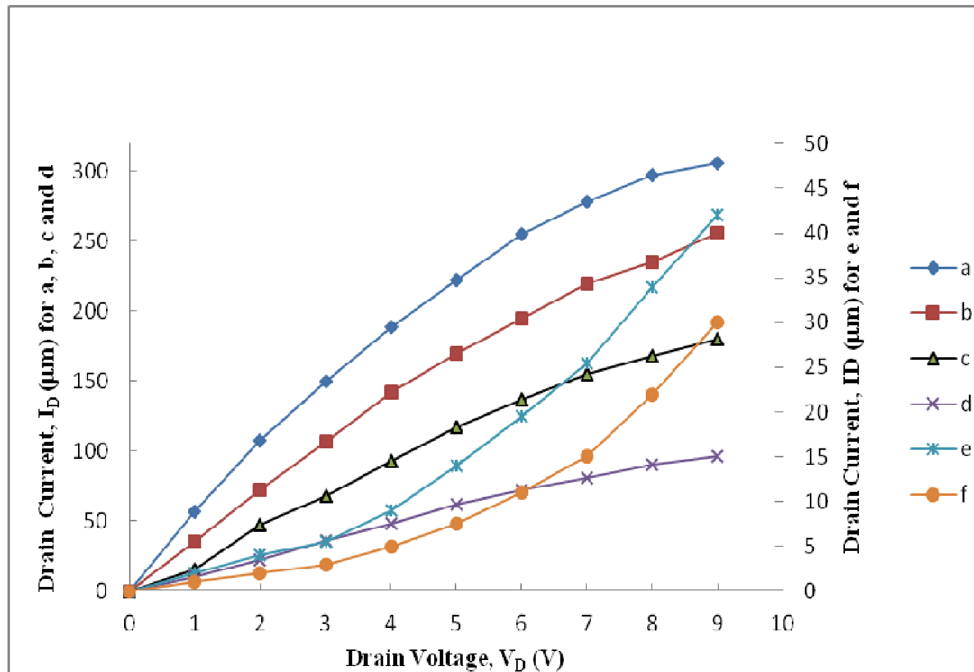

Figure2: Source- drain characteristics of GaAs - Nd_2O_3 TFT at different periods of time

The following transistor parameters are evaluated from the characteristics.
Trans conductance (gm) = 100 μmho.
Output resistance (r_d) = 111 K ohm.
Amplification factor (μ) = 11.1
Gain band-width product = 8.85 KHz

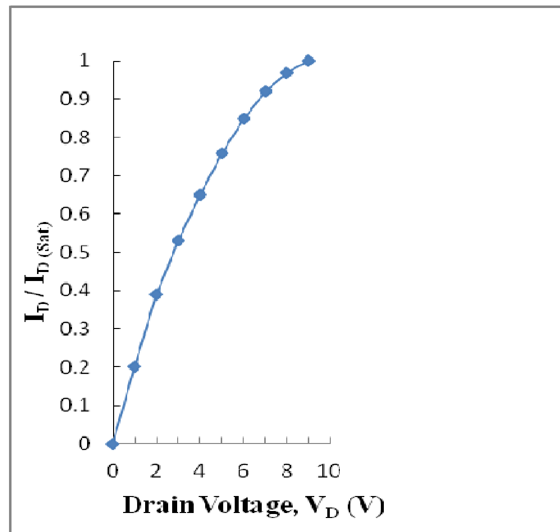

Figure3: Plot of normalized drain current versus drain voltage.

Due to polycrystalline nature of GaAs film, existence of traps in the devices is most common. Moreover, MPD method of fabrication permits entry of contaminants in between deposition

steps. Presence of traps in the devices could be ascertained from Refioglu and De Massa model [8]. According to the authors if the transition of the saturation region of the normalized drain current $I_D/I_{D\,(sat)}$ versus drain voltage plot is sharp the device contains traps. The transition is smoother and less abrupt for trap less TFTs. Relatively sharp transition of this plot at V_G = 5V (fig. 3) infers the presence of traps in the devices.

To assess the trap density the grain boundary trapping model [9] has been used. According to this model the drain current I_D of a TFT with polycrystalline material is given by

$$I_D = w\mu_b(\frac{V_D}{l})C_i V_G \exp(\frac{-q^3 N_t^{\,2} t}{8\in KTC_i}) \qquad (1)$$

Where w and l are the channel width and length, μ_b is the mobility, C_i is the insulator capacitance per unit area, N_t is the trap concentration per unit area and t is the thickness of the semiconductor film.

It is evident from equation (1) that the plot of ln (I_D/V_G) as a function of $1/V_G$ is a straight line from the slope of which N_t can be obtained. From the pre exponential part of equation (1) the value of mobility can be estimated. The departure from linearity of this graph occurs when

$$\frac{N_G}{t} = N_D^*$$

Where $N_G = \frac{C_i}{q} V_G$ and N^*_D is the critical donor density. The crystal size L can be estimated from $N_D^* = \frac{N_t}{L}$. The values of different parameters obtained for the present device are listed below.

Trap density (N_t) = 2.44 x 10^{12} cm^{-2}
Critical donor density (N_D^*) = 2.28 x $10^{18}$$cm^{-3}$
Mobility (μ_b) = 0.37 $cm^2V^{-1}S^{-1}$
Grain size (L) = 107 Å

Figure 1 indicates that GaAs - Nd_2O_3 TFTs exhibit good channel modulation but it is evident from figure 2 that the stability of the devices is poor. The characteristics deteriorate with time and the ambient exposure accelerates the process of deterioration. Significant trapping of charge carriers is also evident from the value of N_t presented above. A high interface trap density at the semiconductor dielectric interface can increase the threshold voltage restricting operation of the TFT at high voltage [10]. The value of mobility of the fabricated devices is also quite low. It might be due to increased surface scattering for the introduction of surface states by atmospheric contamination during exposure of the semiconductor layer prior to the deposition of the oxide film [11]. However, for some applications such as pixel select transistors a modest mobility of ~ 1 $cm^2V^{-1}S^{-1}$ is also adequate [12].

A number of factors are thought to be responsible for device deterioration and collapsing. The oxide used in this investigation though claimed to be 99.9% pure by the manufacturer, may be contaminated with ions which move through the film under the influence of applied electric field. The glass substrates may also contribute towards instability though they are cleaned carefully. In the MPD method of TFT fabrication a layer of air and other atmospheric contaminants might remain trapped in between the semiconductor and the insulator layer. Such a trapped layer might contain sufficient moisture which would help oxidation of the GaAs film and contribute towards the fast states. During ambient exposure of the semiconductor film foreign contaminants both neutral and ionized may also enter the S-I interface. Some contaminants or a layer of air might also be trapped in between the glass substrate and the dielectric film. An absorbed layer may represent a channel both for ion migration and electron migration [13]. During the period of stability investigation these impurities might have slightly diffused in to the GaAs layer to increase the surface states.

Another influencing factor affecting the TFT performance is the nature of s-d contacts. For achieving ideal characteristics the contacts between s-d electrodes and semiconductor film should be ohmic. Though aluminium is known to make a satisfactory ohmic contact with GaAs film, due to ambient exposure of the s-d electrodes prior to the deposition of the GaAs film, a thin insulating barrier air or other contaminants might remain trapped between these two films. Such a barrier would degrade the contact between s-d electrodes and GaAs film. Again the scattering of Al to the s-d gap during electrode deposition would also introduce acceptor like states in the semiconductor film [14]. Oxidation of Al electrodes with time is also responsible for degradation of s-d contacts.

CONCLUSION

TFTs fabricated with the semiconductor insulator combination of GaAs and Nd_2O_3 exhibits good channel modulation but stability is poor. The drain current decreases with time and ambient exposure lead to faster deterioration. Presence of traps and absorption of atmospheric vapour contribute towards device degradation. Improved fabrication technique will be needed to ascertain the suitability of this semiconductor insulator combination.

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